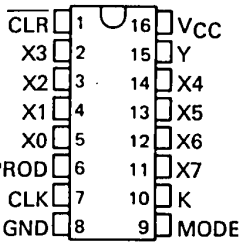
TYPES SN54LS384, SN74LS384
8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

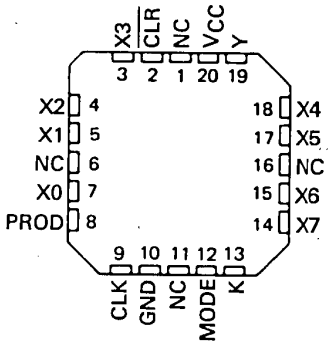
D2419, JANUARY 1981 – REVISED DECEMBER 1983

- Two's-Complement Multiplication
- Magnitude Only Multiplication
- Cascadable for Any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 40 MHz Typical Maximum Clock Frequency

SN54LS384 . . . J PACKAGE
SN74LS384 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS384 . . . FK PACKAGE
SN74LS384 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'LS384 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to produce a two's-complement product without external correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled via the clear input. When the clear input is low, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is high, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the PROD output, least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an (m + n)-bit product. The 'LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The PROD output of one device is connected to the K input of the succeeding device when cascading. The mode input is used to indicate which device contains the most significant bit. The mode input is wired high or low depending on the position of the 8-bit slice in the total X word length. The device with the most significant bit is wired low and all lower order bit packages are wired high.

The SN54LS384 will be characterized for operation over the full military temperature range from –55°C to 125°C. The SN74LS384 will be characterized for operation from 0°C to 70°C.

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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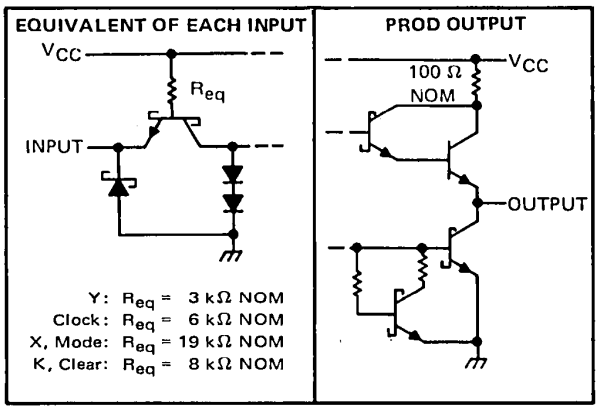
FUNCTION TABLE

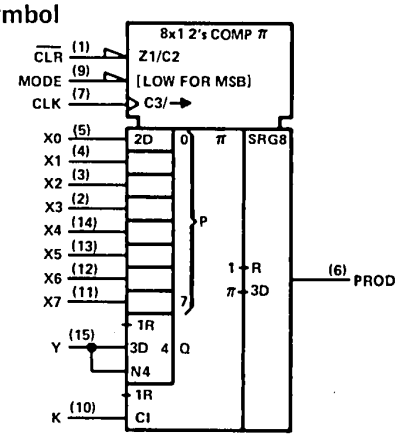
INPUTS				INTERNAL	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	X_i	Y	Y_{-1}	PROD	
L	X	Data	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	↑	X	L	L	Output	Shift sum register
H	↑	X	L	H	per	Add multiplicand to sum register and shift
H	↑	X	H	L	Booth's	Subtract multiplicand from sum register and shift
H	↑	X	H	H	algorithm	Shift sum register

H = high-level, L = low-level, X = irrevelant, ↑ = low-to-high-level transition

schematics of inputs and outputs

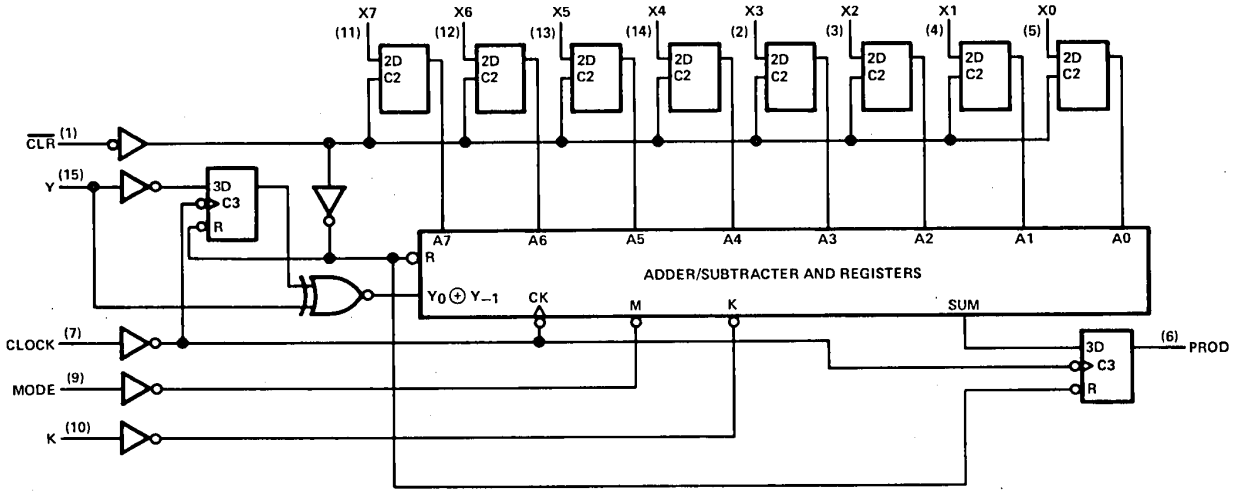


logic symbol



Pin numbers shown on logic notation are for J or N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS384 . . . . . −55°C to 125°C
SN74LS384 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

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recommended operating conditions

		SN54LS384			SN74LS384			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Setup time, t_{su}	Y before Clock ↑	45			38			ns
	K before Clock ↑	30			24			
	X before Clear ↑	23			19			
Clear inactive-state set up time before Clock ↑		30			20			ns
Hold time, t_h	Y after Clock ↑	0			0			ns
	K after Clock ↑	0			0			
	X after Clear ↑	2			2			
Pulse width, t_w	Clock high	20			20			ns
	Clock low	20			20			
	Clear low	38			33			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS384			SN74LS384			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	X, Mode	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		K, Clear						30			30	
		Clock						40			40	
		Y						80			80	
I_{IL}	Low-level input current	X, Mode	V_{CC} = MAX,	V_I = 0.4 V				−0.48			−0.48	mA
		K, Clear						−1.2			−1.2	
		Clock						−1.6			−1.6	
		Y						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3			91	155		91	155	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Note 4	25	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			15	23	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			15	23	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			17	25	ns

NOTE 4: See General Information Section for load circuits and voltage waveforms.

TYPICAL APPLICATION DATA

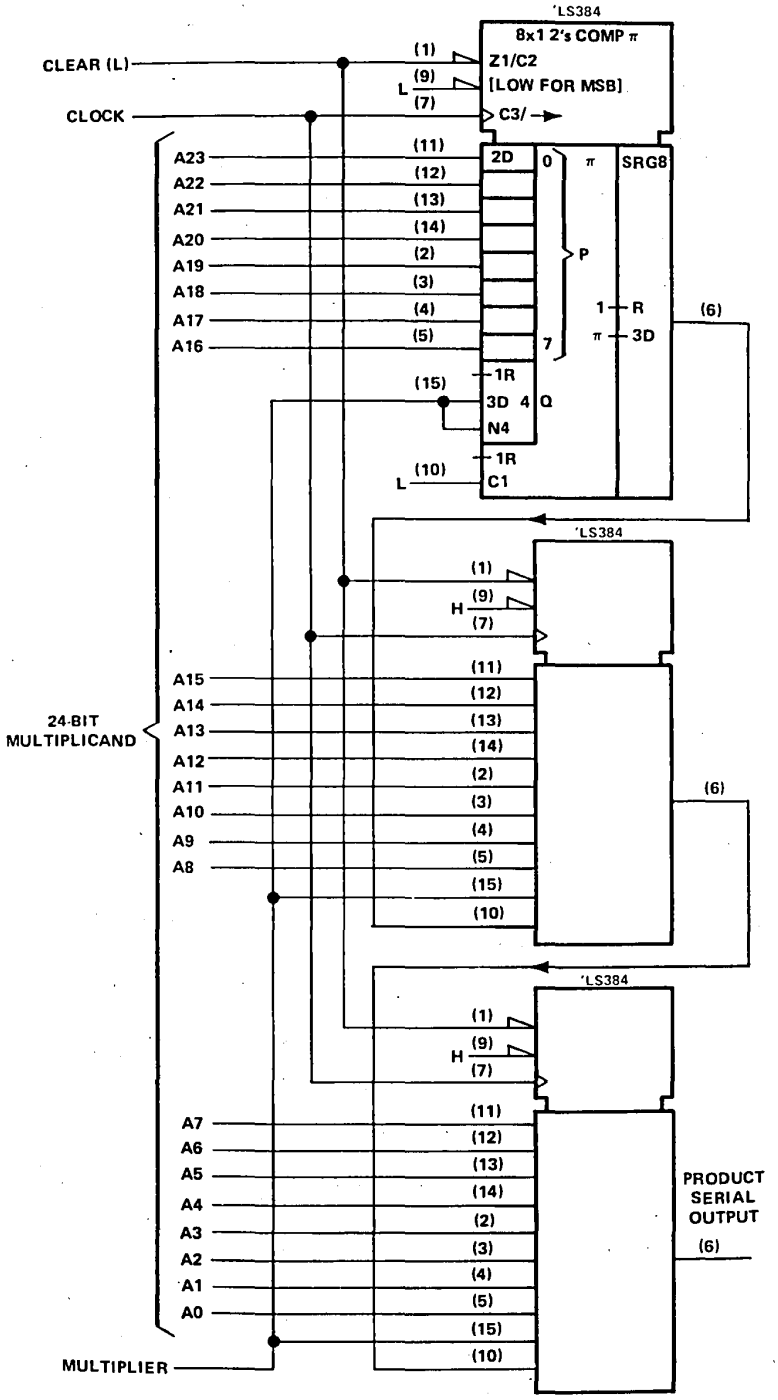

FIGURE 1–BASIC 24-BIT SERIAL/PARALLEL CONNECTION

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TYPICAL APPLICATION DATA

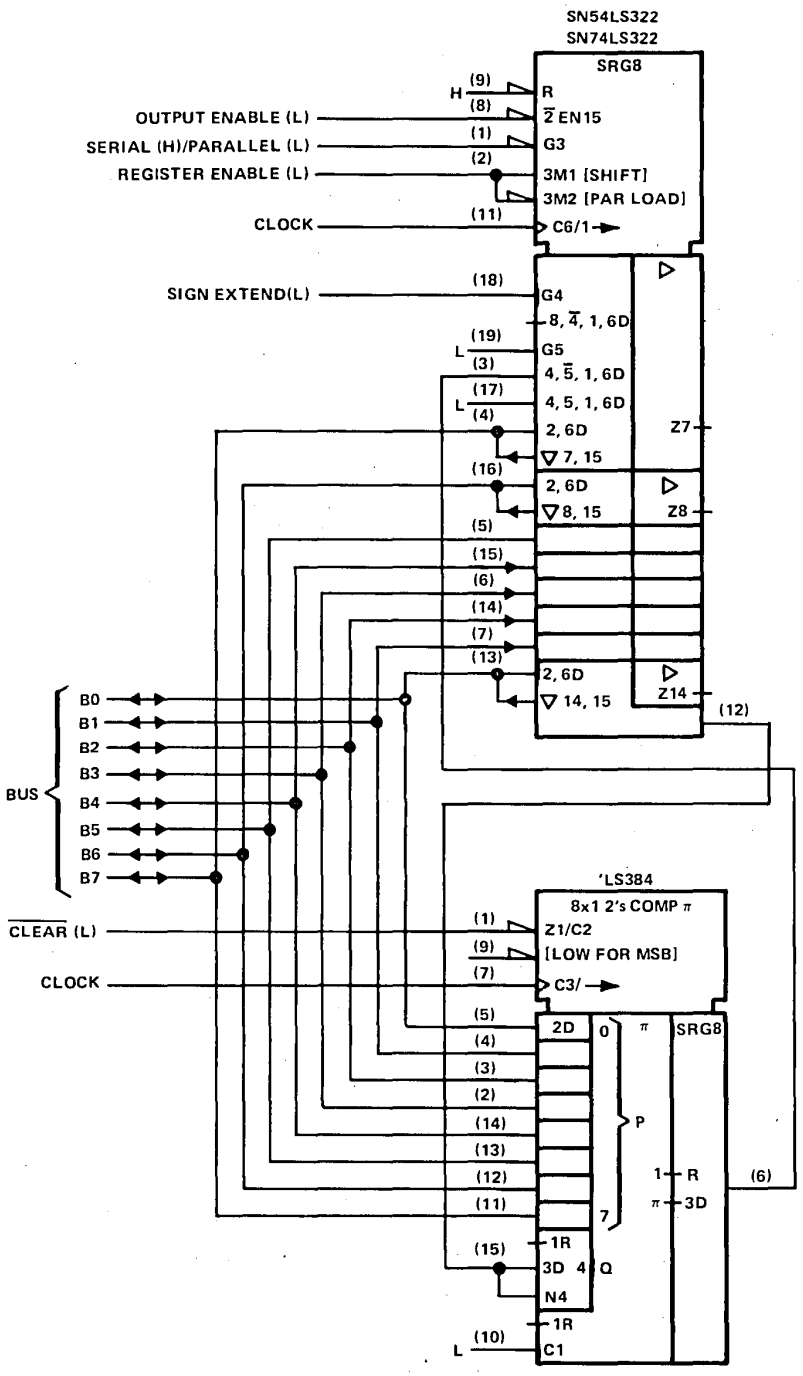

FIGURE 2–8-BIT BY 8-BIT MULTIPLIER, BUS ORGANIZED, WITH 8-BIT TRUNCATED PRODUCT