MOTOROLA

SN54LS/74LS716
SN54LS/74LS718

PROGRAMMABLE MODULO-N COUNTERS

LOW POWER SCHOTTKY

DESCRIPTION — These monolithic devices are programmable, cascadable, modulo-N-counters. The SN54LS/74LS716 can be programmed to divide by any number (N) from 0 thru 9, the SN54LS/74LS718 from 0 thru 15.

The parallel enable ($\overline{PE}$) input enables the parallel data inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

All Types:

Input Loading Factor:
- Clock, $\overline{PE}$ = 2
- D0, D1, D2, D3, Gate = 1
- $\overline{MR}$ = 4

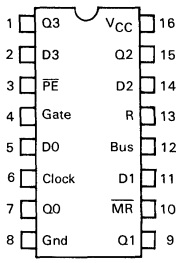
Output Loading Factor = 8

Total Power Dissipation = 85 mW typ/pkg

Propagation Delay Time:
- Clock to Q3 = 50 ns typ
- Clock to Bus = 35 ns typ

CONNECTION DIAGRAM
DIP (TOP VIEW)

V_{CC} = Pin 16
Gnd = Pin 8



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

SN54LS/74LS716

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

SN54LS/74LS718

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

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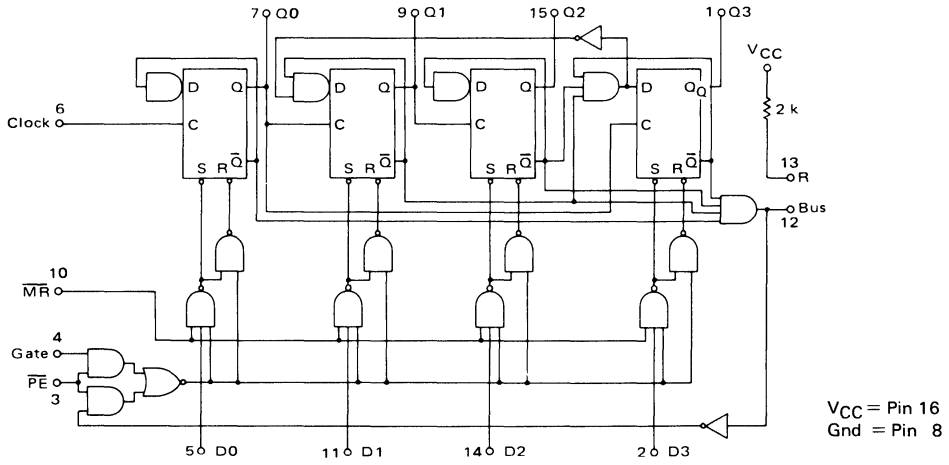
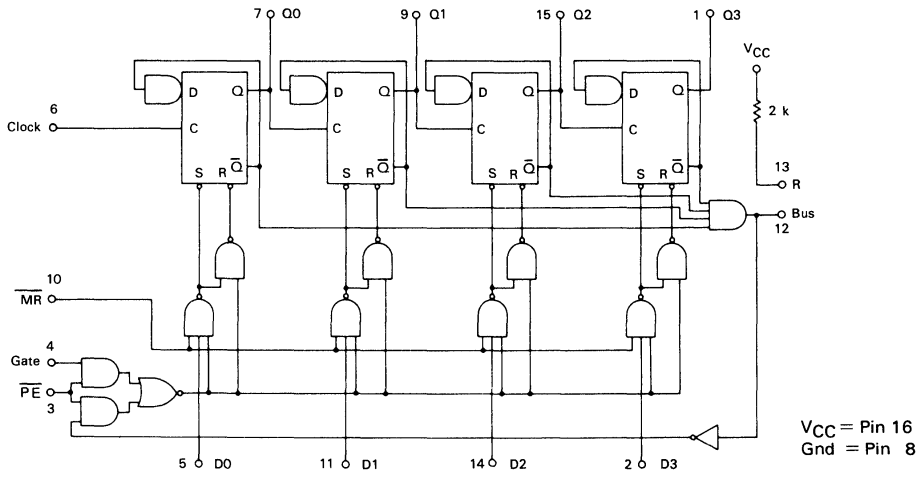
LOGIC DIAGRAMS

SN54LS/74LS716



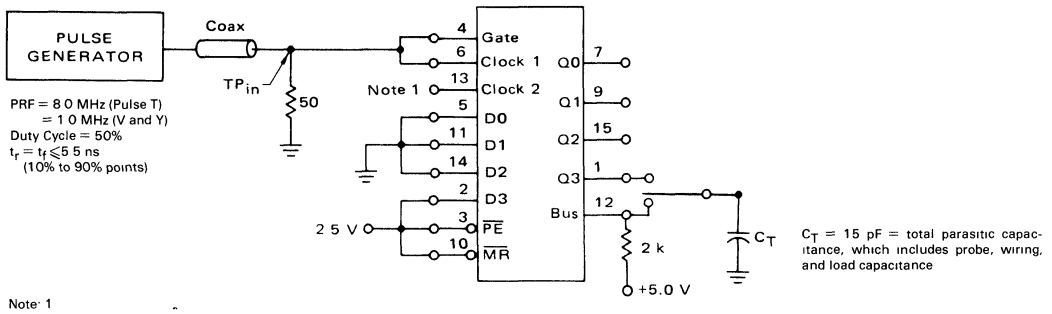
VCC = Pin 16
Gnd = Pin 8

SN54LS/74LS718

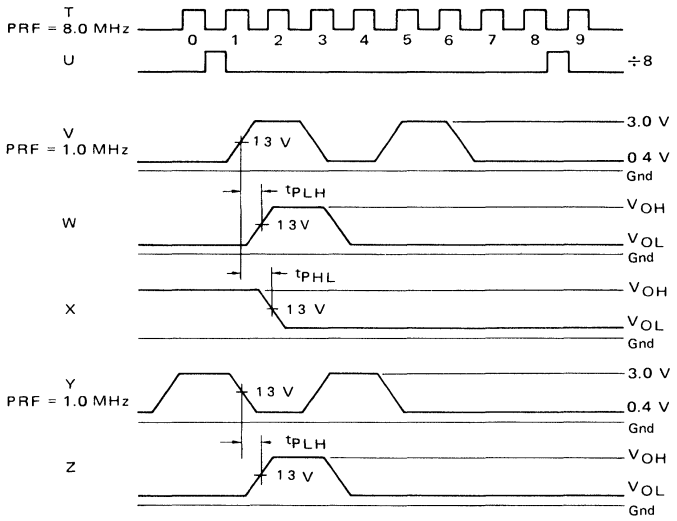


VCC = Pin 16
Gnd = Pin 8

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



Note 1
Counter programmed for ÷8 operation, Pin 13 is the resistor pin, and left open



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				OUTPUT		LIMITS		
		Clock Pin 6	Gate Pin 4	D0, D1, D2 Pins 5, 11, 14	D3, $\overline{PE}$, $\overline{MR}$ Pins 2, 3, 10	Bus Pin 12	Q3 Pin 1	Min	Max	Unit
Toggle Frequency (Check before measuring propagation delay.)	f_{tog}	T	T	Gnd	2.5 V	—	U	8.0	—	MHz
Propagation Delay Clock to Bus	t_{PLH}	V	V	Gnd	2.5 V	W	—	—	65	ns
Propagation Delay Gate to Q3	t_{PLH}	Y	Y	Gnd	2.5 V	—	Z	—	35	ns
Propagation Delay Clock 1 to Q3	t_{PHL}	V	V	Gnd	2.5 V		X			
SN54LS/74LS716								—	45	ns
SN54LS/74LS718								—	78	ns

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
I_{IH}	Input HIGH Current Data, Clock, Gate Enable $\overline{MR}$				20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Data, Clock, Gate Enable $\overline{MR}$				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current Data, Clock, Gate Enable $\overline{MR}$				−0.4 −0.8 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current	Others	−30		−130	mA	V_{CC} = MAX
		R Output	−1.8		−3.8	mA	
I_{CC}	Power Supply Current			17	32	mA	V_{CC} = MAX

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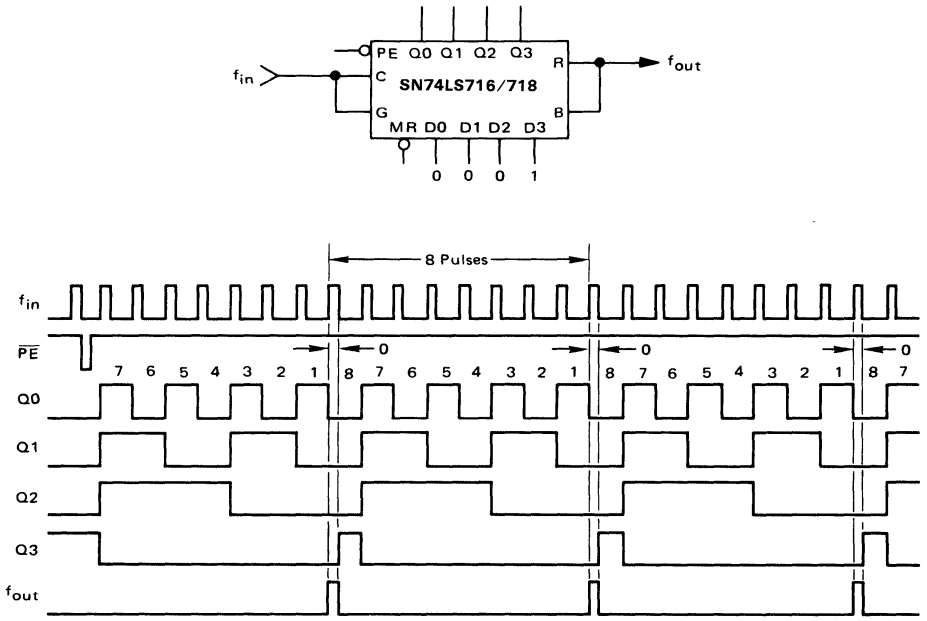

Fig. 1 — SINGLE-STAGE OPERATION

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OPERATING CHARACTERISTICS

Operation of both counters is essentially the same. The SN54LS/74LS716 has a maximum modulus of ten while the SN54LS/74LS718 is capable of dividing by up to sixteen. Minor differences in the programming procedure will be covered in the discussion of cascaded stages.

Suitable connections for operating a single stage are shown in Figure 1, as well as appropriate waveforms. The desired modulus is applied to the data inputs D0, D1, D2, and D3 in binary SN74LS718 or binary coded decimal SN74LS716 positive logic format. If a number greater than nine (BCD 1001) is applied to the SN74LS716 it treats the most significant bit position as a zero; if for example, binary fourteen (1110) were applied to an SN74LS716 the counter would divide by six. BCD eight is programmed in Figure 1. As $\overline{PE}$ is taken low the states on the parallel inputs are transferred to their respective outputs. Subsequent positive transitions of the input clock will decrement the counter until the all zero state is detected by the bus gate. The resulting positive transition of the bus line is internally inverted and fed back to the preset gating circuitry but does not yet preset the counter since the gate-clock input is still high. As the clock returns to the low state the counter is set to the programmed state, taking the bus line low. The net result is one positive pulse on the bus line for every N clock pulses. The output pulse width is approximately equal to one clock pulse high time.

Operation will continue in this fashion until the data on the programmable inputs is changed. Since the preset circuitry is inhibited except when the counter is in the zero state, preset data may be changed while clocking is occurring. If it is necessary to enter a new number before the counter has reached zero this can be done by momentarily taking $\overline{PE}$ low. Countdown will continue from the new number on the next positive clock transition.

The counters can be made to divide by 10 (SN74LS716) or 16 (SN74LS718) by inhibiting the preset logic. This may be done by either holding the gate input high or by holding the bus line low.

The normal connections for cascading stages are indicated in Figure 2, with the appropriate waveforms. Note that the gate input of each stage is connected to the clock; all bus outputs are tied to one of the internal pullup resistors, R. The total modulus for cascaded SN74LS716's is determined from $N_T = N_0 + 10N_1 + 100N_2 + \ldots$; N_T for SN74LS718's is given by $N_T = N_0 + 16N_1 + 256N_2 + \ldots$ Stated another way, the BCD equivalent of each decimal digit is applied to respective SN74LS716 stages while the data inputs of the SN74LS718 stages are treated as part of one long binary number. The difference in programming is illustrated in Figure 2 where $N_T = 245$ is coded for both counter types.

Cascaded operation can be further clarified by referring to the timing diagram of Figure 2. For the SN74LS716 counting begins with the first positive clock transition after the data has been set in. After the five clock pulses, the least-significant stage has been counted down to zero. The bus line does not go high at this time since the three bus terminals are wire-ORed and the other two stages are not in the zero state. Since no reset occurs, the next positive clock edge advances the least significant stage to the nine (1001) state, causing the second stage to be decremented. The process continues in this manner with the least significant stage now dividing by ten. The second stage eventually counts down to zero and also reverts to dividing by ten. Each pulse out of the second stage decrements the third until it reaches zero. At this time the bus line goes high; it remains high until the clock goes low, causing all three stages to be reset to the programmed count again.

Maximum operating frequency of the basic SN74LS716/718 counter is limited by the time required for reprogramming at the end of each count down cycle. Operation can be extended to approximately 25 MHz by adding an "early decode" feature as shown in Figure 3. The appropriate connections for three stages are shown; however up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all Parallel Enables are connected to the $\overline{Q}$ output of a type D flip-flop formed by gates G1 through G6; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input to the flip-flop. Four additional data inputs are provided for decoding the "two" state of the least significant stage. Circuit operation is illustrated in the waveforms of Figure 3 where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 applied. Timing is now shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached. This condition causes the remaining D inputs to the flip-flop to be high. The next-to-last clock pulse of the cycle then triggers the flip-flop Q output high. $\overline{Q}$ simultaneously takes the parallel enable of all stages low, resetting the programmed data to the outputs. The next input pulse clocks Q (f_{out}) back to the zero stage, since the data inputs to the flip-flop are no longer all high. The positive output pulse is one input clock period in duration. Note that division by N equal to 1 or 2 is not available using this method.

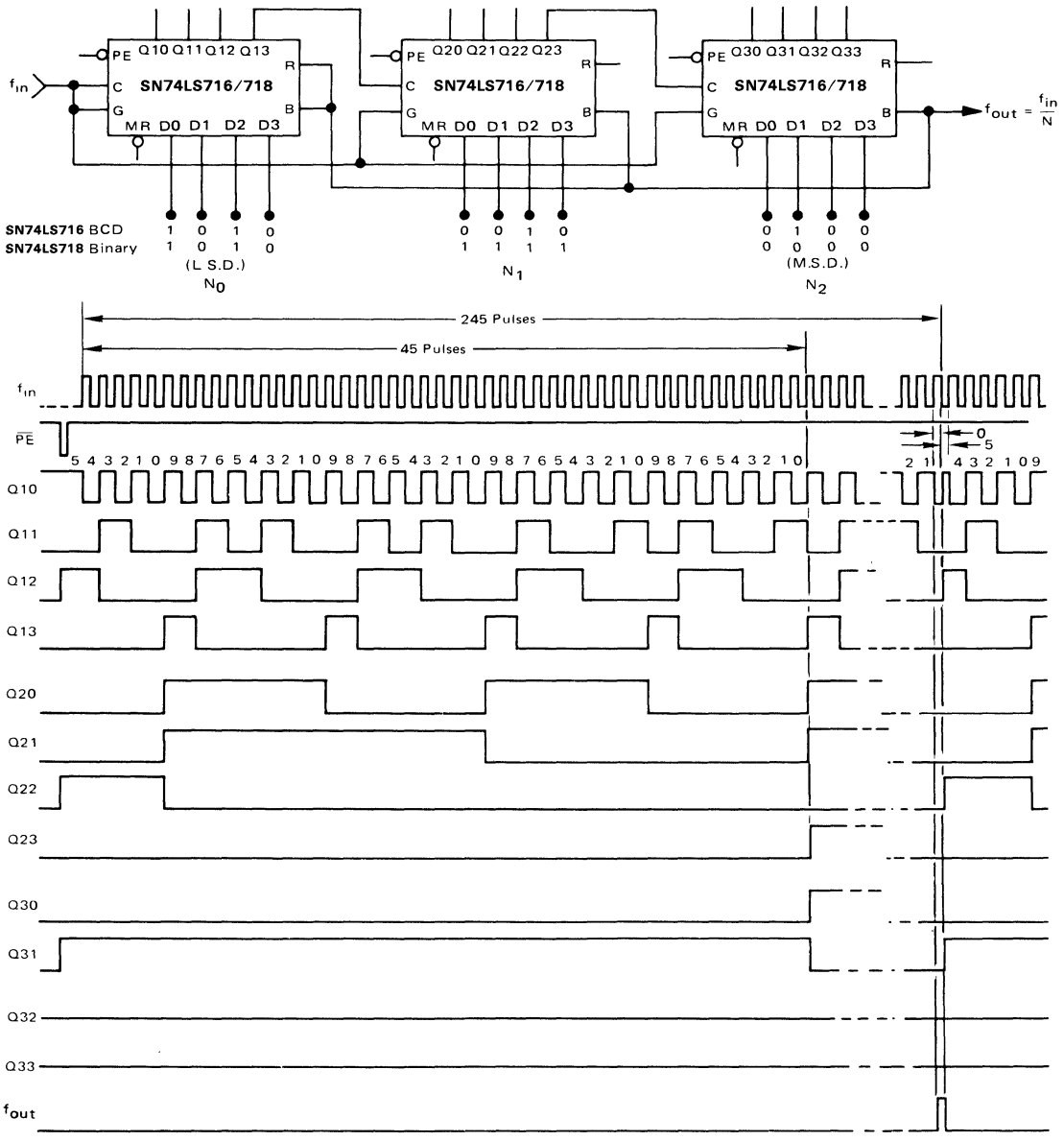

Fig. 2 — CASCADED OPERATION

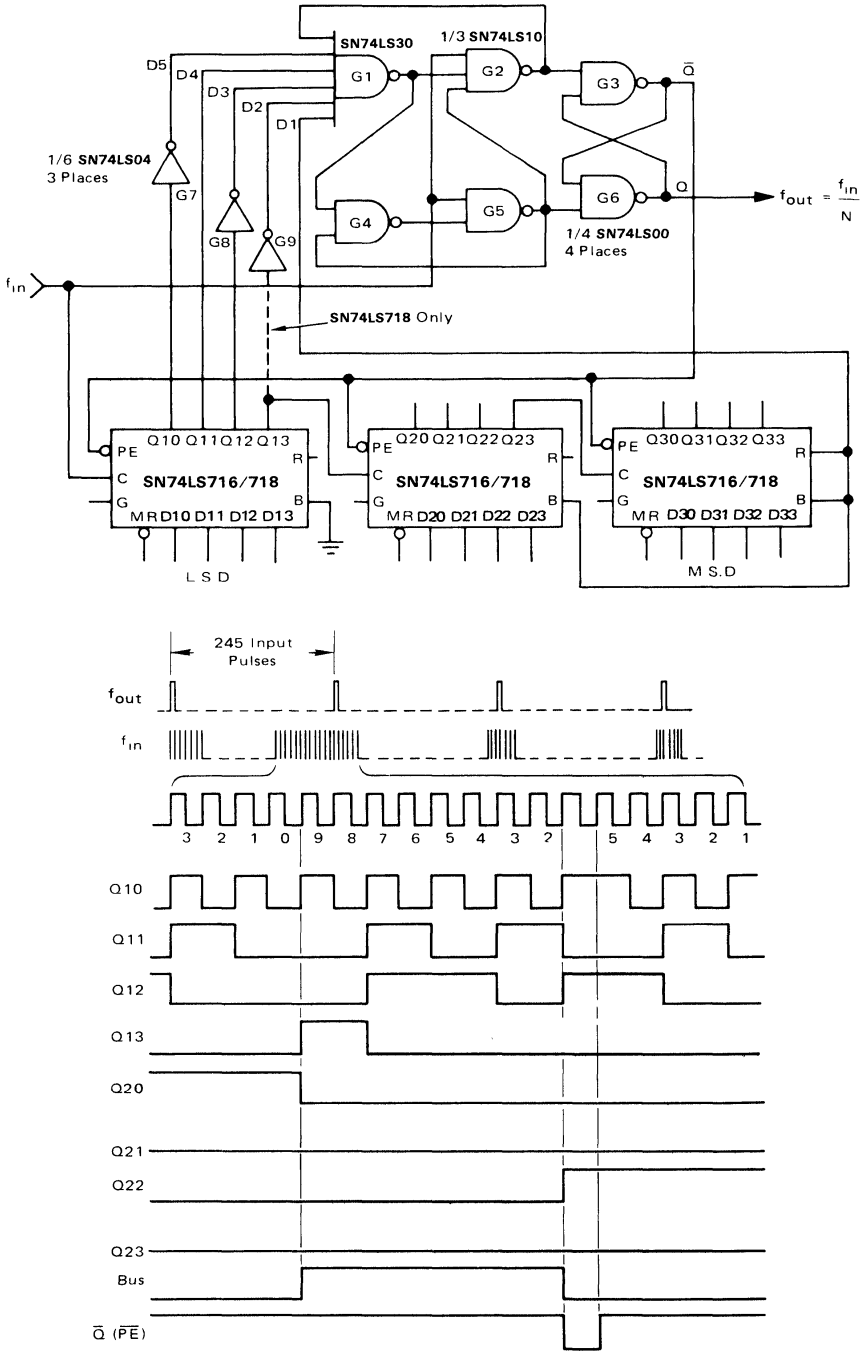

Fig. 3 — INCREASING OPERATING RANGE

APPLICATIONS INFORMATION

A typical system application for programmable counters is illustrated in the frequency synthesizer shown in Figure 4. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[1] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divided-by-M ECL circuit as shown in Figure 5. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 5, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 6.[2]. It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the

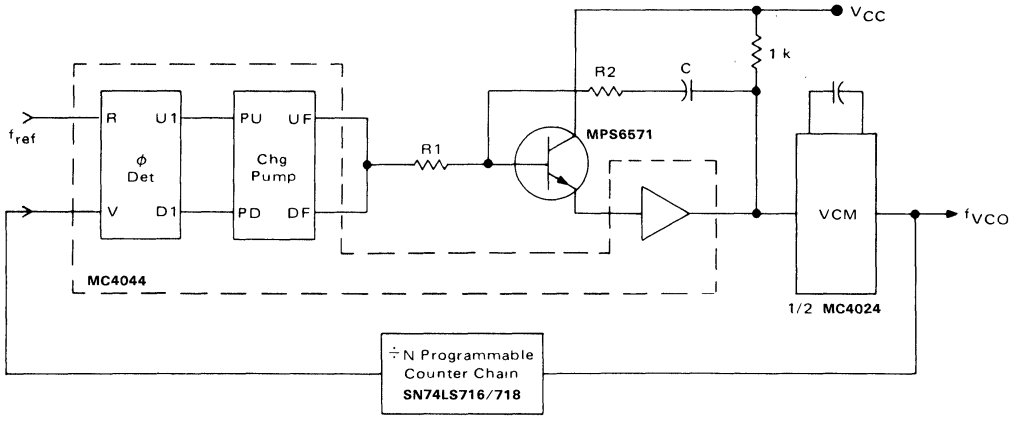

Fig. 4 — MTTL PHASE-LOCKED LOOP

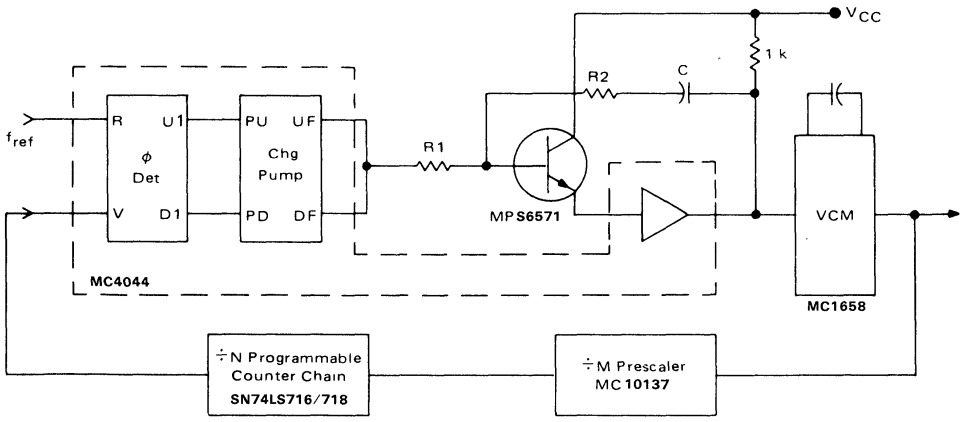

Fig. 5 — MTTL-MECL PHASE-LOCKED LOOP

1 See Motorola Application Note AN-535 and the MC4344/4044 Data Sheet for detailed explanation of overall circuit operation

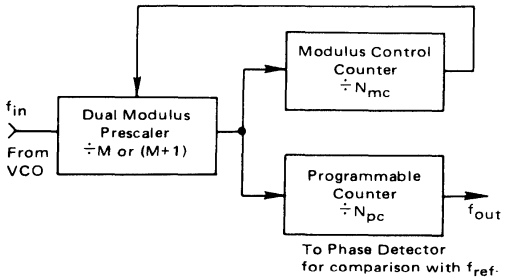

Fig. 6 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER

programmable counter for division by N_{pc}. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle. For this configuration,

$$f_{out} = \frac{f_{in}}{MN_{pc}+N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})\, f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

A simplified example of this technique is shown in Figure 7. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 as shown in Figure 7. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain.

A specific example of this technique is shown in Figure 8. There the feedback divider circuitry required for generating frequencies between the 144 MHz and 178 MHz with 30 kHz channel spacing is shown.[2]

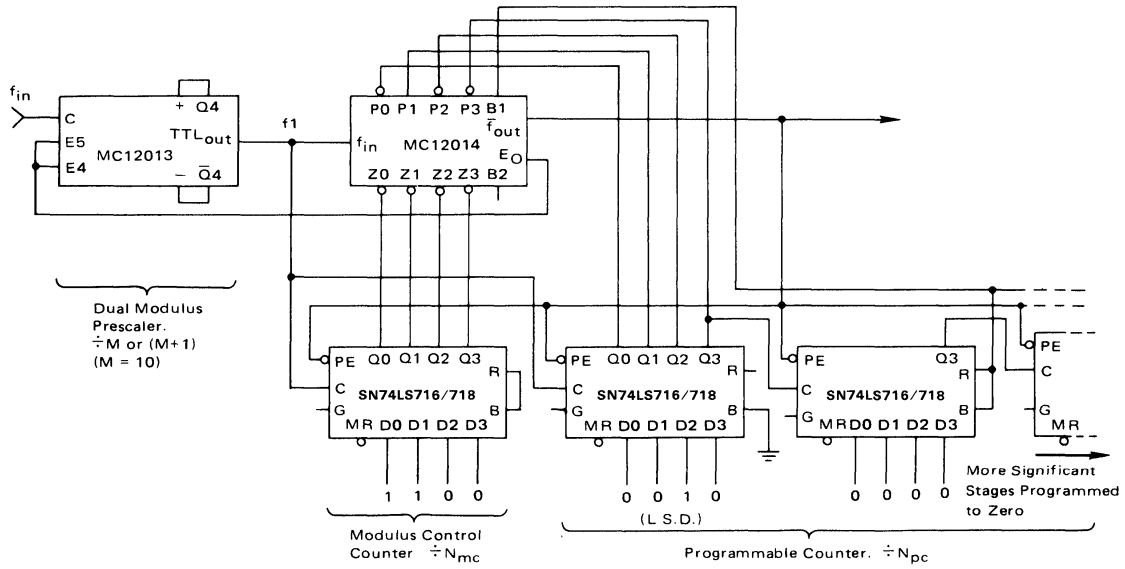

Fig. 7 — FREQUENCY DIVISION: $f_O = f_{in}/MN_{pc} = N_{mc}$

2. This application is discussed in greater detail in the MC 12014 Counter Control Logic data sheet.

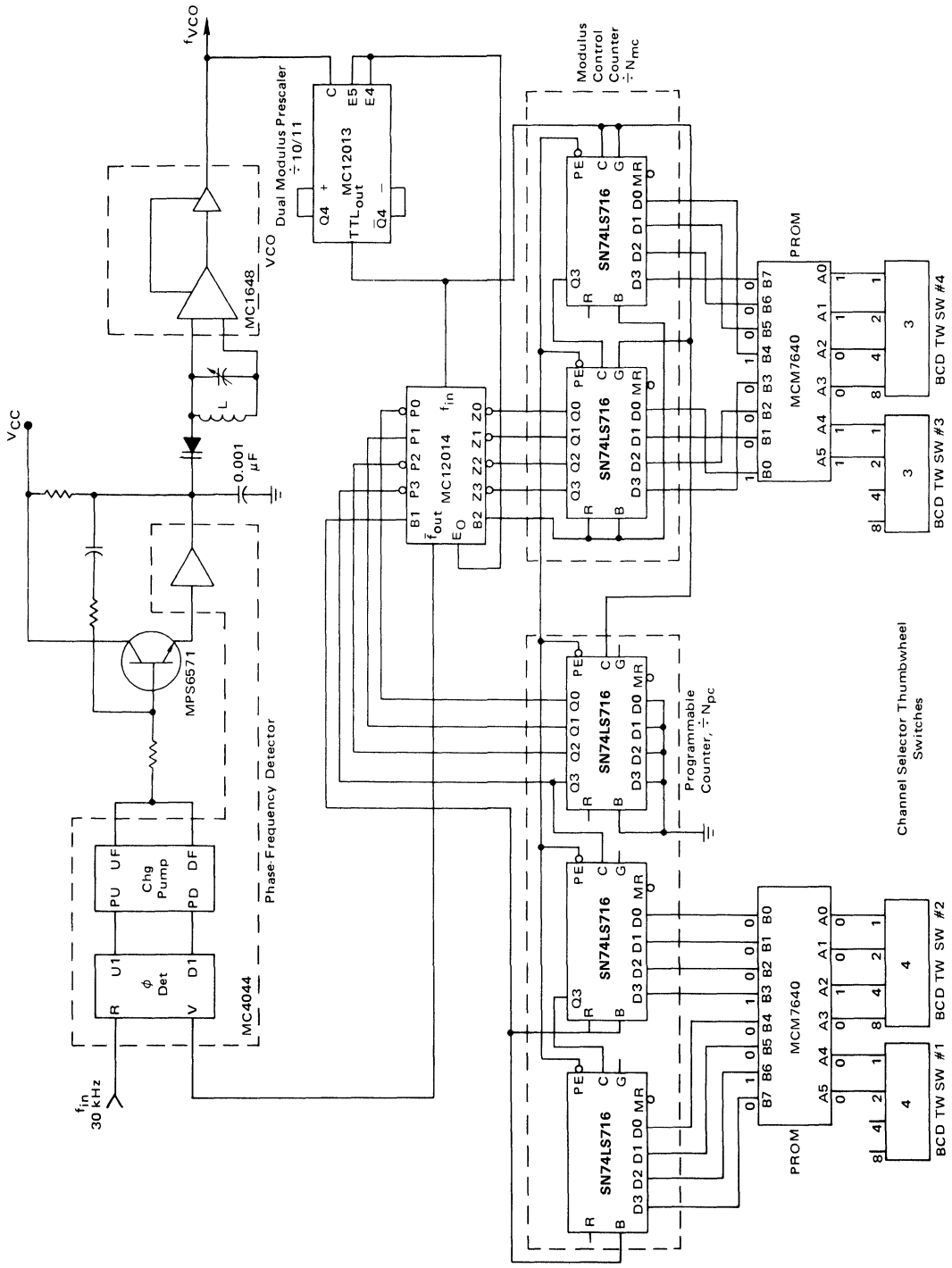

Fig. 8 — 144 to 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING