'LS668 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS669 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Buffered Outputs

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS668, 'LS669	32 MHz	32 MHz	100 mW

SN54LS668, SN54LS669 . . . J PACKAGE
SN74LS668, SN74LS669 . . . D, J OR N PACKAGE
(TOP VIEW)

```
        U/D̄ [ 1  ⌄ 16 ] V_CC
        CLK [ 2    15 ] RCO
          A [ 3    14 ] Q_A
          B [ 4    13 ] Q_B
          C [ 5    12 ] Q_C
          D [ 6    11 ] Q_D
        ENP [ 7    10 ] ENT̄
        GND [ 8     9 ] LOAD
```

SN54LS668, SN54LS669 . . . FK PACKAGE
SN74LS668, SN74LS669 . . . FN PACKAGE
(TOP VIEW)

```
         CLK  U/D̄  NC  V_CC  RCO
          3    2    1   20   19
     A [ 4              18 ] Q_A
     B [ 5              17 ] Q_B
    NC [ 6              16 ] NC
     C [ 7              15 ] Q_C
     D [ 8              14 ] Q_D
          9   10  11  12  13
         ENP GND  NC LOAD ENT̄
```

NC − No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.
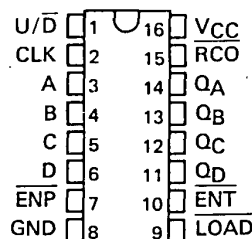
These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse when the count is maximum counting up or zero counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.
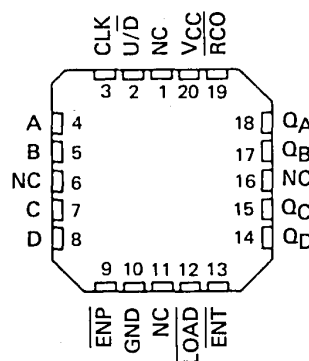
These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time, reduced input currents I_{IH} and I_{IL}, and all buffered outputs.

TTL DEVICES

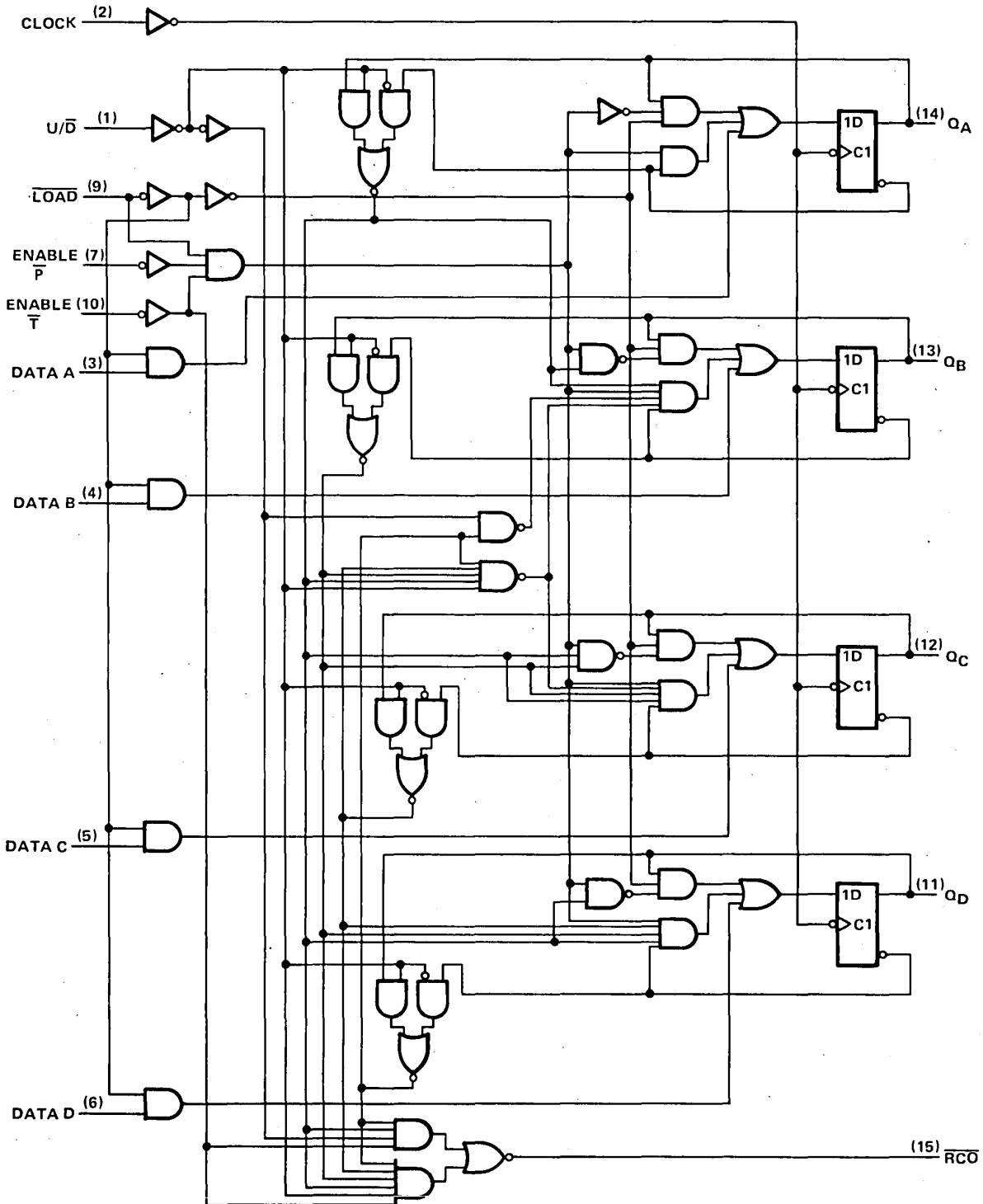**TEXAS INSTRUMENTS**
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265
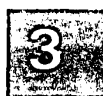
TYPES SN54LS668, SN74LS668
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS
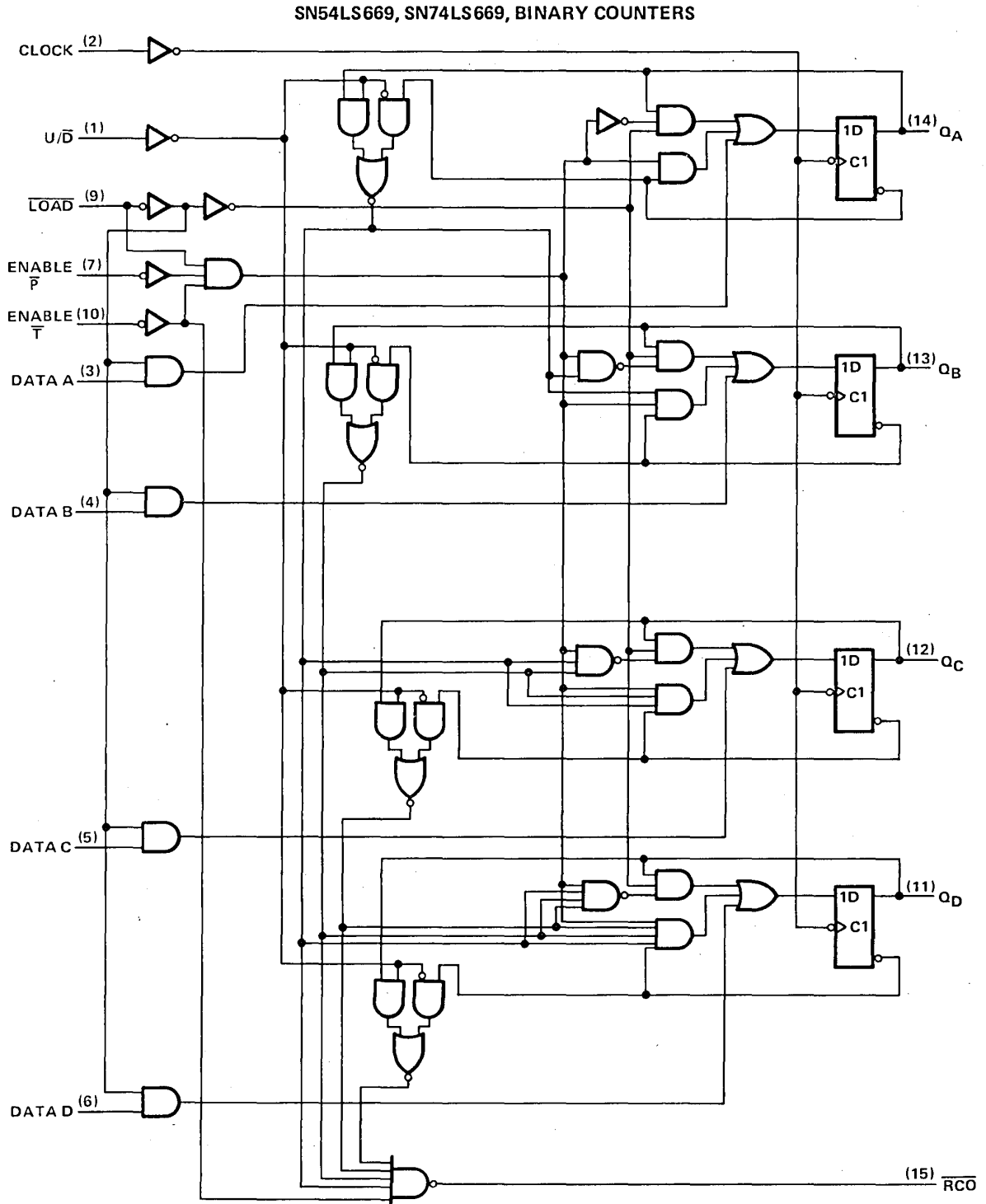
logic diagram

SN54LS668, SN74LS668, DECADE COUNTERS

Pin numbers shown on logic notation are for D, J or N packages.

logic diagram (continued)

SN54LS669, SN74LS669, BINARY COUNTERS

Pin numbers shown on logic notation are for D, J or N packages.

'LS668 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

logic symbol

Pin numbers shown on logic notation are for D, J or N packages.

TEXAS
INSTRUMENTS
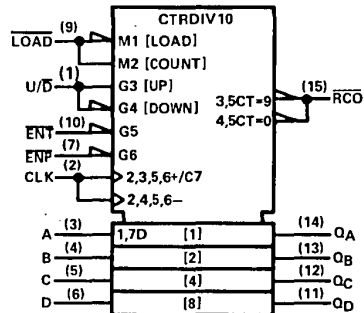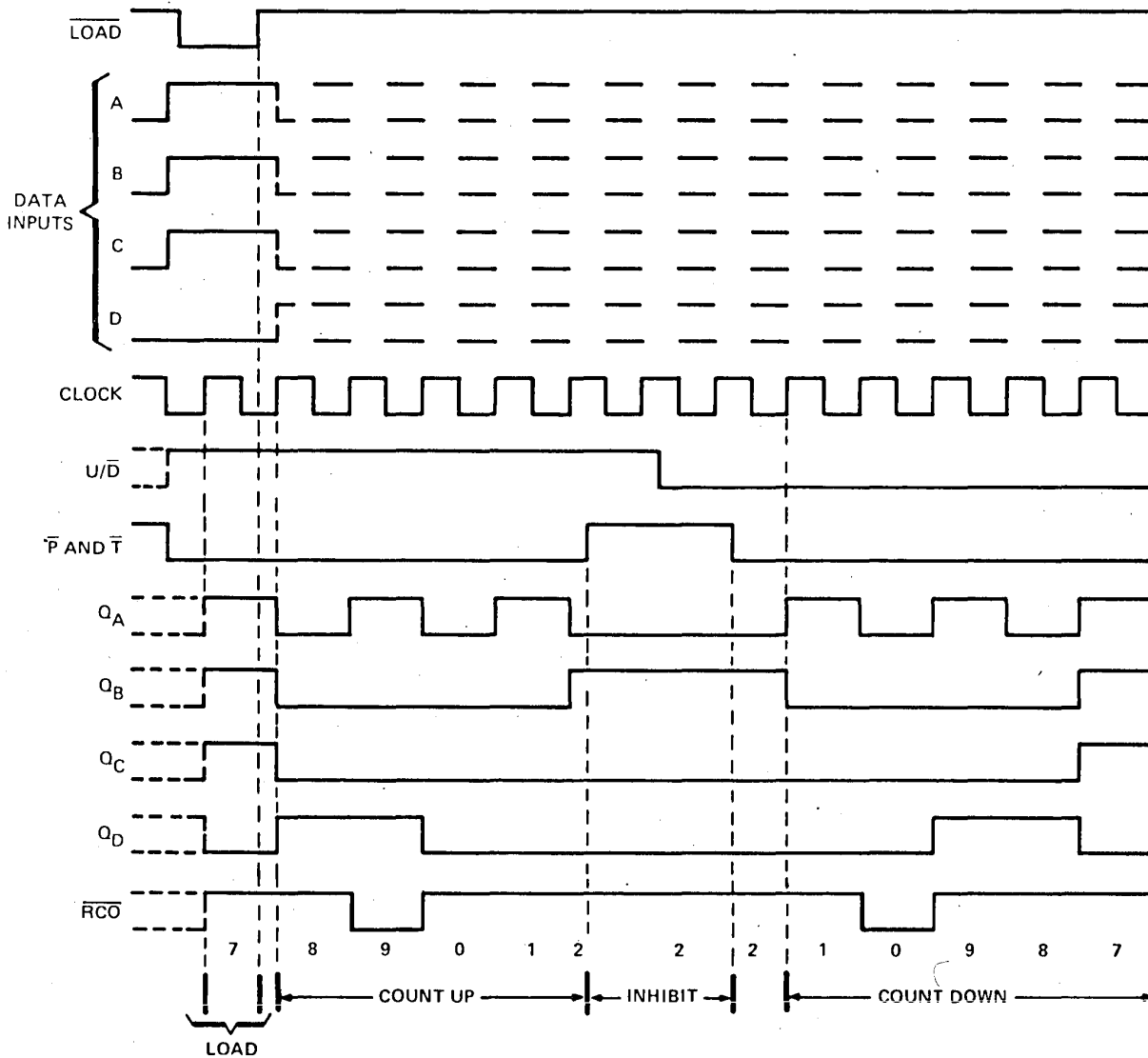POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

3

TTL DEVICES

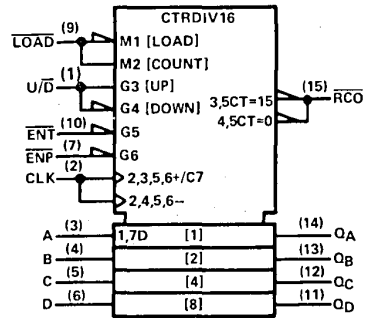## 'LS669 BINARY COUNTERS

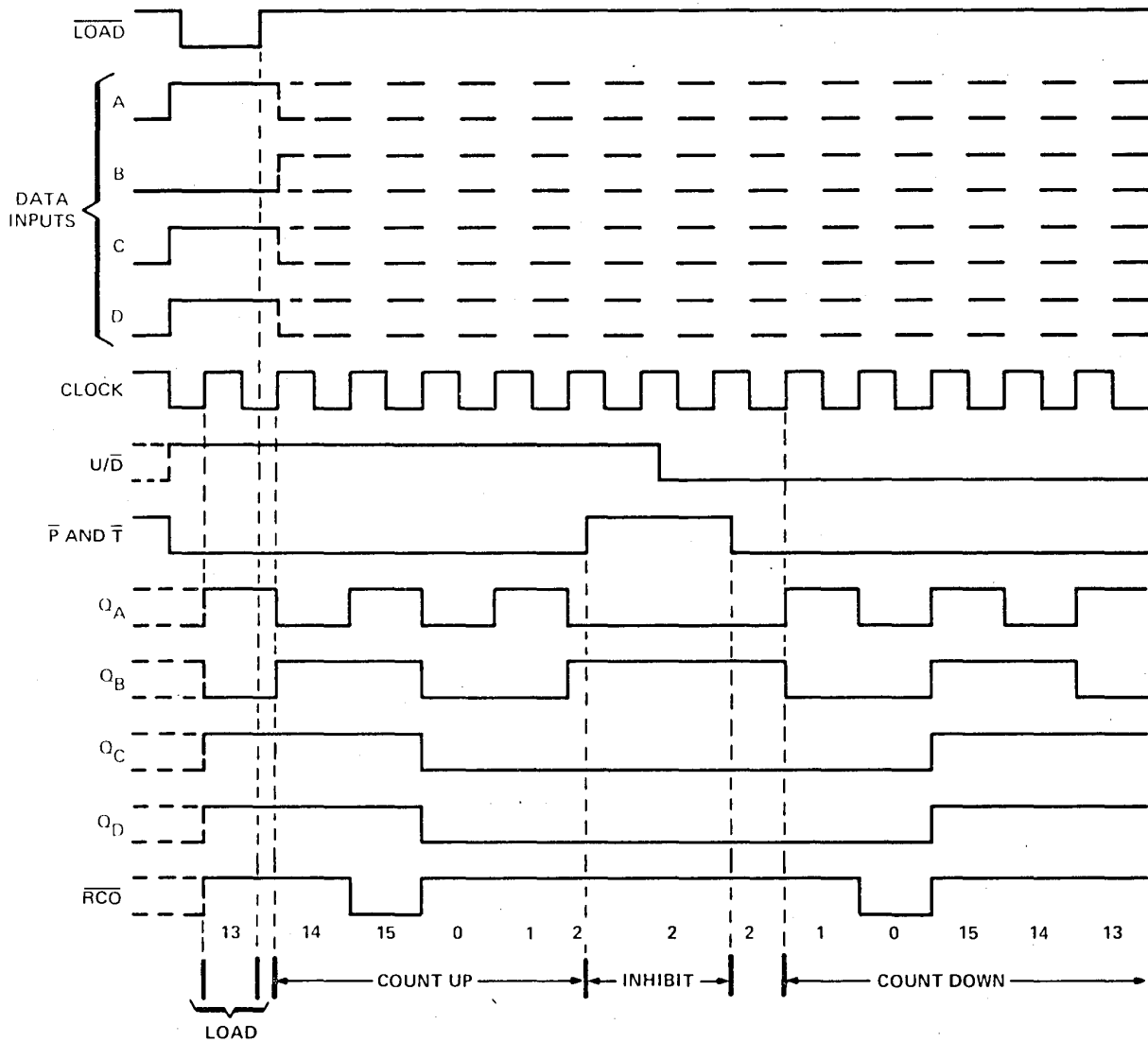### typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen
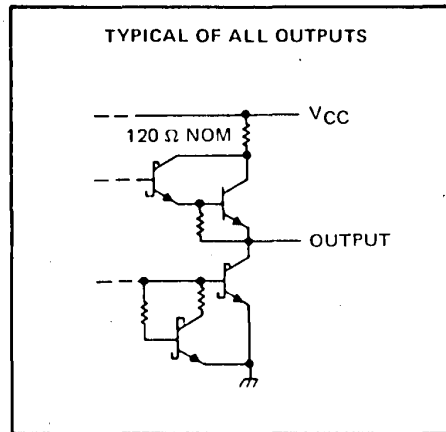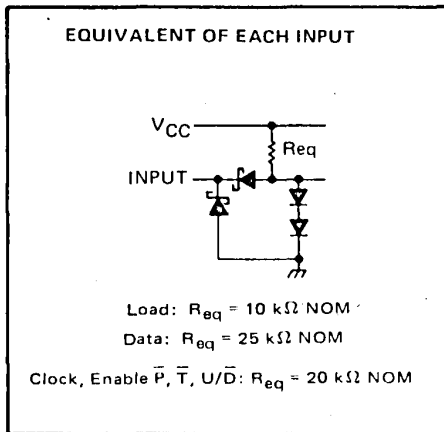
logic symbol

Pin numbers shown on logic notation are for D, J or N packages.

TTL DEVICES

3

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

V_{CC}

R_{eq}

INPUT

Load: R_{eq} = 10 kΩ NOM

Data: R_{eq} = 25 kΩ NOM

Clock, Enable $\overline{P}$, $\overline{T}$, U/$\overline{D}$: R_{eq} = 20 kΩ NOM

TYPICAL OF ALL OUTPUTS

V_{CC}

120 Ω NOM

OUTPUT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 7 V
Operating free-air temperature range: SN54LS668, SN54LS669 . . . . −55°C to 125°C
                                                            SN74LS668, SN74LS669 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1)		20			20			ns
Setup time, t_{su} (see Figure 1)	Data inputs A, B, C, D	25			25			ns
	$\overline{ENP}$ or $\overline{ENT}$	40			40			
	$\overline{LOAD}$	30			30			
	U/$\overline{D}$	45			45			
Hold time at any input with respect to clock, t_h (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 µA	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max / I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	A, B, C, D, P̄, U/D̄	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
	Clock, T̄				0.1			0.1	
	LOAD				0.2			0.2	
I_{IH} High-level input current	A, B, C, D, P̄, U/D̄	V_{CC} = MAX, V_I = 2.7 V			20			20	µA
	Clock, T̄				20			20	
	LOAD				40			40	
I_{IL} Low-level input current	A, B, C, D, P̄, U/D̄	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	Clock, T̄				−0.4			−0.4	
	LOAD				−0.8			−0.8	
I_{OS} Short-circuit output current[§]		V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 2		20	34		20	34	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	32		MHz
t_{PLH}	CLK	RCO			26	40	ns
t_{PHL}					40	60	
t_{PLH}	CLK	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Figures 2 and 3		18	27	ns
t_{PHL}					18	27	
t_{PLH}	ENT	RCO			11	17	ns
t_{PHL}					29	45	
t_{PLH}◇	U/D̄	RCO			22	35	ns
t_{PHL}◇					26	40	

[¶]f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
◇Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.
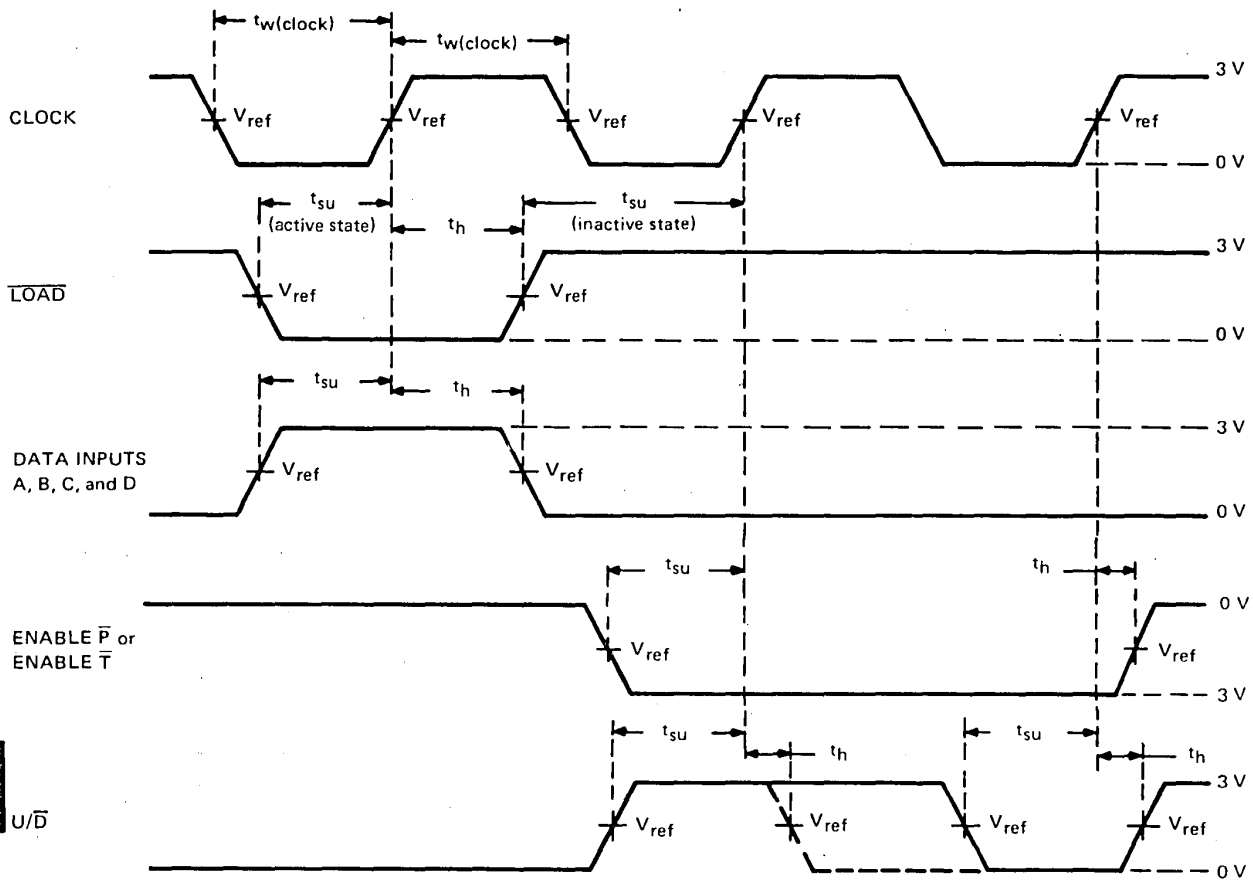
TTL DEVICES 3

PARAMETER MEASUREMENT INFORMATION

$t_{w(clock)}$

CLOCK V_{ref} V_{ref} V_{ref} V_{ref} V_{ref} 3 V / 0 V

t_{su} (active state) t_h t_{su} (inactive state)

$\overline{LOAD}$ V_{ref} V_{ref} 3 V / 0 V

t_{su} t_h

DATA INPUTS A, B, C, and D V_{ref} V_{ref} 3 V / 0 V

t_{su} t_h

ENABLE $\overline{P}$ or ENABLE $\overline{T}$ V_{ref} V_{ref} 0 V / 3 V

t_{su} t_h t_{su} t_h

U/$\overline{D}$ V_{ref} V_{ref} V_{ref} V_{ref} 3 V / 0 V

VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR $\leqslant$ 1 MHz, duty cycle $\leqslant$ 50%, $Z_{out} \approx$ 50 Ω; $t_r \leqslant$ 15 ns, $t_f \leqslant$ 6 ns.

B. V_{ref} = 1.3 V.

FIGURE 1—PULSE WIDTHS, SETUP TIMES, HOLD TIMES

ENABLE $\overline{T}$ V_{ref} V_{ref} 3 V / 0 V

t_{PHL} t_{PLH}

$\overline{RCO}$ V_{ref} V_{ref} V_{OL} / V_{OH}

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR $\leqslant$ 1 MHz, duty cycle $\leqslant$ 50%, $Z_{out} \approx$ 50 Ω; $t_r \leqslant$ 15 ns, $t_f \leqslant$ 6 ns.

B. t_{PLH} and t_{PHL} from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'LS668, all Q outputs high for 'LS669).

C. V_{ref} = 1.3 V.

D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668, or 15 for 'LS669) the ripple carry output will be out of phase.

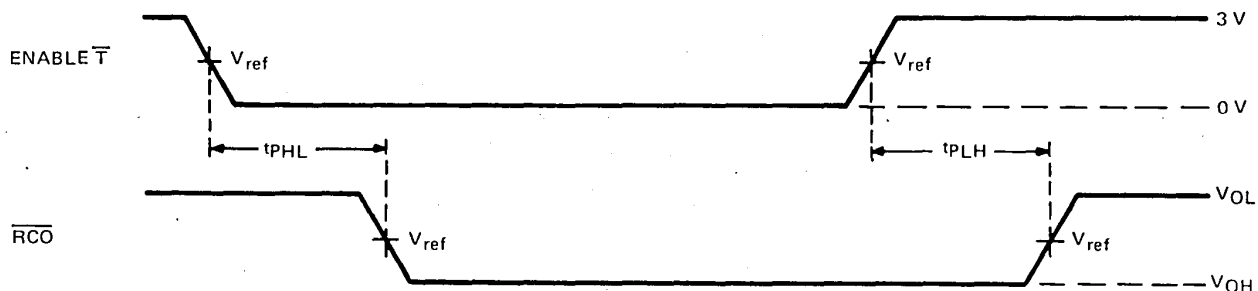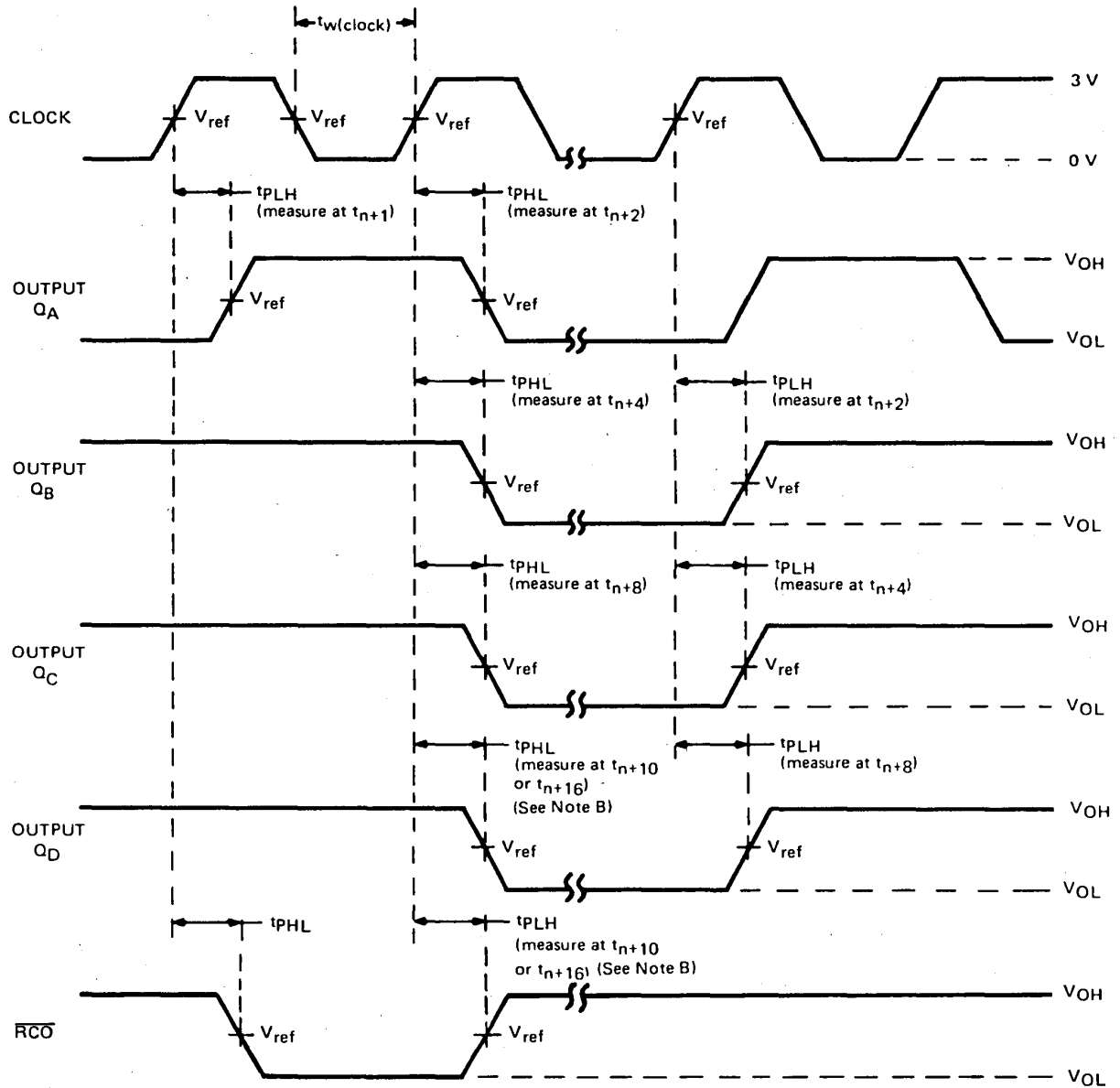### FIGURE 2—PROPAGATION DELAY TIMES TO CARRY OUTPUT

PARAMETER MEASUREMENT INFORMATION

UP-COUNT VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50 \, \Omega$, $t_r ≤ 15$ ns, $t_f ≤ 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the 'LS668, and at t_{n+16} for the 'LS669, where t_n is the bit-time when all outputs are low.

C. $V_{ref} = 1.3$ V.

FIGURE 3—PROPAGATION DELAY TIMES FROM CLOCK

TTL DEVICES

3