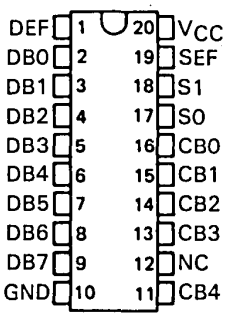
TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637
8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

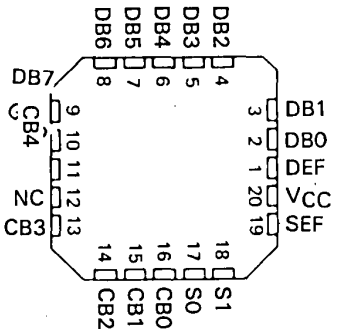
D2728, APRIL 1983, REVISED DECEMBER 1983

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Fast Processing Times:**
  - **Write Cycle: Generates Check Word in 45 ns Typical**
  - **Read Cycle: Flags Errors in 27 ns Typical**
- **Power Dissipation 500 mW Typical**
- **Choice of Output Configurations:**
  - **'LS636 . . . 3-State**
  - **'LS637 . . . Open Collector**

SN54LS' . . . J PACKAGE
SN74LS' . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS' . . . FK PACKAGE
SN74LS' . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

description

The 'LS636 and 'LS637 devices are 8-bit parallel error detection and correction circuits (EDACs) in 20-pin, 300-mil packages. They use a modified Hamming code to generate a 5-bit check word from an 8-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 13-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 8-bit data word are flagged and corrected.

Single-bit errors in the 5-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 8-bit word is not in error. The correction cycle will simply pass along the original 8-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

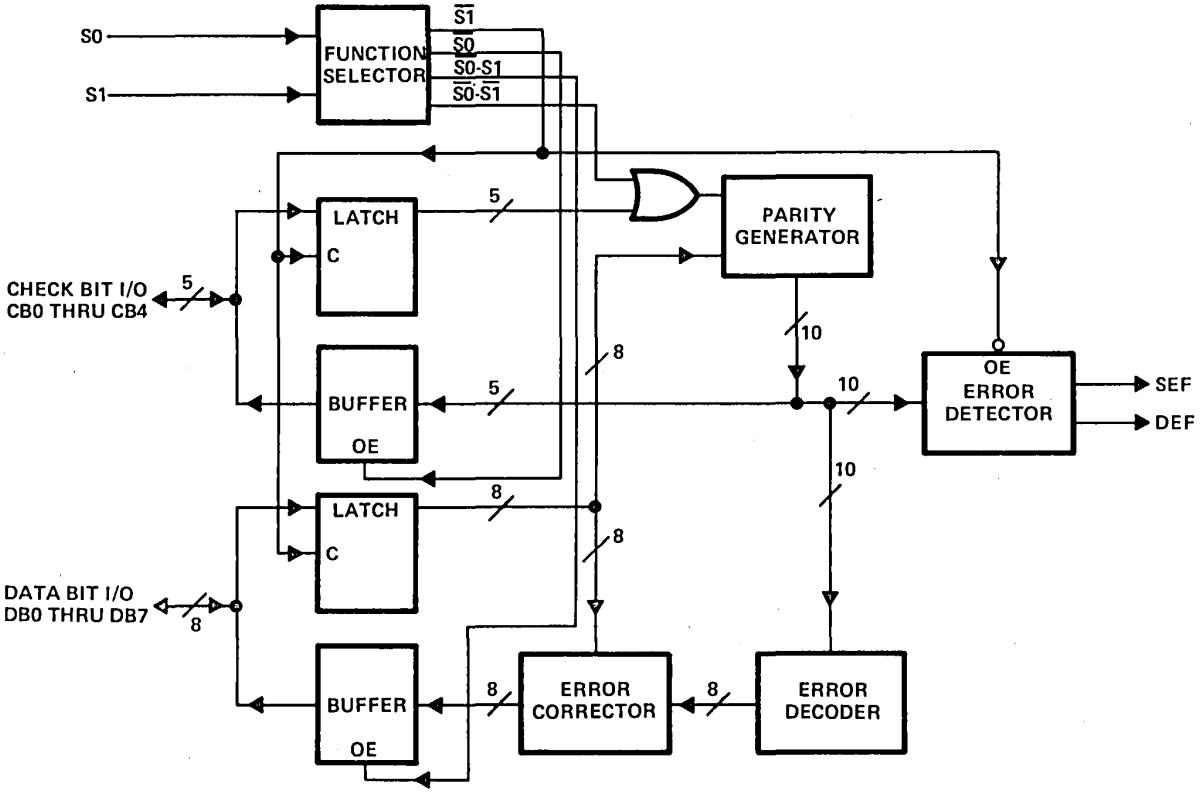
Dual-bit errors are flagged but not corrected. These dual errors may occur in any two bits of the 13-bit word from memory (two errors in the 8-bit data word, two errors in the 5-bit check word, or one error in each word).

The gross-error condition of all highs from memory will be detected. Otherwise, errors in three or more bits of the 13-bit word are beyond the capabilities of these devices to detect.

CONTROL FUNCTION TABLE

MEMORY CYCLE	CONTROL		EDAC FUNCTION	DATA I/O	CHECK WORD I/O	ERROR FLAGS	
	S1	S0				SEF	DEF
WRITE	L	L	Generate Check Word	Input Data	Output Check Word	L	L
READ	L	H	Read Data & Check Word	Input Data	Input Check Word	L	L
READ	H	H	Latch & Flag Errors	Latch Data	Latch Check Word	Enabled	
READ	H	L	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	

functional block diagram



ERROR FUNCTION TABLE

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA
8-BIT DATA	5-BIT CHECKWORD	SEF	DEF	CORRECTION
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 8-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

error detection and correction details

During a memory write cycle, five check bits (CB0-CB4) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 5-bit check word is retrieved along with the 8-bit data word.

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CHECKWORD BIT	8-BIT DATA WORD							
	0	1	2	3	4	5	6	7
CB0	X	X		X	X			
CB1	X		X	X		X	X	
CB2		X	X		X	X		X
CB3	X	X	X				X	X
CB4				X	X	X	X	X

The five check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

Error detection is accomplished as the 5-bit check word and the 8-bit data word from memory are applied to internal parity generators/checkers. If the parity of all five groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 8-bit data word will change the sense of exactly three bits of the 5-bit check word. Any single error in the 5-bit check word changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

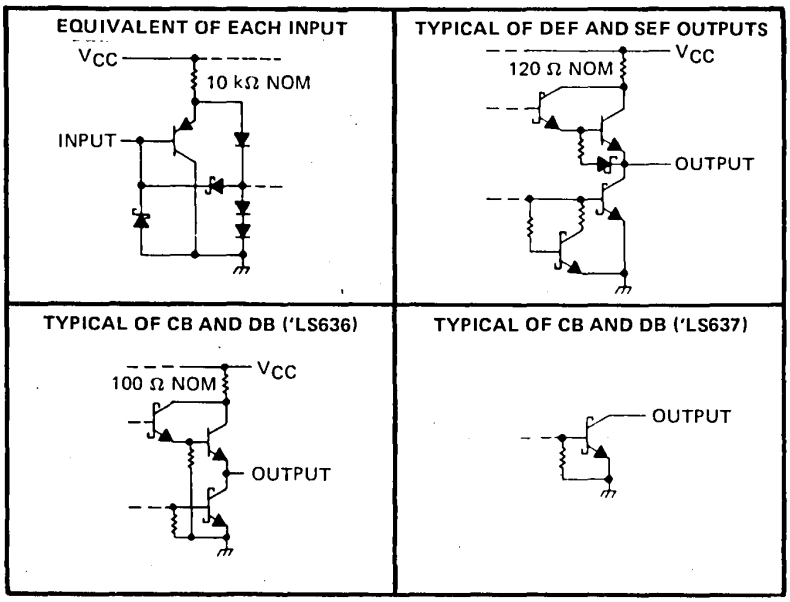
Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 8-bit data word and 5-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the check word I/O port presents a 5-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

ERROR SYNDROME TABLE

ERROR LOCATION	SYNDROME ERROR CODE				
	CB0	CB1	CB2	CB3	CB4
DB0	L	L	H	L	H
DB1	L	H	L	L	H
DB2	H	L	L	L	H
DB3	L	L	H	H	L
DB4	L	H	L	H	L
DB5	H	L	L	H	L
DB6	H	L	H	L	L
DB7	H	H	L	L	L
CB0	L	H	H	H	H
CB1	H	L	H	H	H
CB2	H	H	L	H	H
CB3	H	H	H	L	H
CB4	H	H	H	H	L
NO ERROR	H	H	H	H	H

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: S0 and S1 . . . . . 7 V
CB and DB . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS636, SN54LS637 . . . . . −55°C to 125°C
SN74LS636, SN74LS637 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS636 SN54LS637			SN74LS636 SN74LS637			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	CB or DB, 'LS636 only			−1			−1	mA
		DEF or SEF			−0.4			−0.4	
V_{OH}	High-level output voltage	CB or DB, 'LS637 only			5.5			5.5	V
I_{OL}	Low-level output current	CB or DB			12			24	mA
		DEF or SEF			4			8	
t_{su}	Setup time	CB or DB before S1↑†	15			15			ns
		CB or DB before S1↑‡	45			45			
t_h	Hold time	CB or DB after S1↑	15			15			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

† This time guarantees the input data and checkword will be latched.
‡ This time guarantees the input data and checkword will be latched plus that no glitch will occur on SEF or DEF flags.
↑ The upward-pointing arrow indicates a transition from low to high.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS			TEST CONDITIONS†		SN54LS636 MIN	SN54LS636 TYP‡	SN54LS636 MAX	SN74LS636 MIN	SN74LS636 TYP‡	SN74LS636 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} min	I_{OH} = MAX	2.4	3.3		2.4	3.2		V
		DEF or SEF		I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		DEF or SEF		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	CB or DB	V_{CC} = MAX, S0 and S1 at 2 V	V_O = 2.7 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	CB or DB	V_{CC} = MAX, S0 and S1 at 2 V	V_O = 0.4 V,			−0.2			−0.2	mA
I_I	Input current at maximum input voltage	CB or DB	V_{CC} = MAX, V_{IH} = 4.5 V	V_I = 5.5 V			0.1			0.1	mA
		S0 or S1		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}§	Short-circuit output current	CB or DB	V_{CC} = MAX		−30		−130	−30		−130	mA
		DEF or SEF			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, S0 and S1 at 4.5 V, All CB and DB pins grounded, DEF and SEF open			100	160		100	160	mA

PARAMETER			TEST CONDITIONS†		SN54LS637 MIN	SN54LS637 TYP‡	SN54LS637 MAX	SN74LS637 MIN	SN74LS637 TYP‡	SN74LS637 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	DEF or SEF	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = −400 μA, V_{IL} = V_{IL} max	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current	CB or DB	V_{CC} = MIN, V_{IH} = 2 V,	V_{OH} = 5.5 V, V_{IL} = V_{IL} max			0.1			0.1	mA
V_{OL}	Low-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		DEF or SEF		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	CB or DB	V_{CC} = MAX, V_{IH} = 4.5 V	V_I = 5.5 V			0.1			0.1	mA
		S0 or S1		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}§	Short-circuit output current	DEF or SEF	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, S0 and S1 at 4.5 V, All CB and DB grounded, SEF and DEF open			90	144		90	144	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

'LS636 switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS636 MIN	'LS636 TYP	'LS636 MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output◇	DB	CB	S0 at 0 V, S1 at 0 V, R_L = 667 Ω, See Figure 1		31	45	ns
t_{PHL} Propagation delay time, high-to-low-level output◇					45	65	ns
t_{PLH} Propagation delay time, low-to-high-level output*	S1↑	DEF	S0 at 3 V, R_L = 2 kΩ, See Figure 1		27	40	ns
		SEF			20	30	
t_{PZH} Output enable time to high level#	S0↓	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 2		24	40	ns
t_{PZL} Output enable time to low level#	S0↓	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 1		30	45	ns
t_{PHZ} Output disable time from high level▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 2		43	65	ns
t_{PLZ} Output disable time from low level▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 1		31	45	ns

'LS637 switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF, see Figure 1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS637 MIN	'LS637 TYP	'LS637 MAX	UNIT
t_{PLH} Propagation delay time, low-to-high level output◇	DB	CB	S0 at 0 V, S1 at 0V, R_L = 667 Ω		38	55	ns
t_{PHL} Propagation delay time, high-to-low-level output◇					45	65	ns
t_{PLH} Propagation delay time, low-to-high-level output*	S1↑	DEF	S0 at 3 V, R_L = 2 kΩ		27	40	ns
		SEF			20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output#	S0↓	CB, DB	S1 at 3 V, R_L = 667 kΩ		28	45	ns
t_{PLH} Propagation delay time, low-to-high-level output▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 kΩ		33	50	ns

◇These parameters describe the time intervals taken to generate the check word during the memory write cycle.
*These parameters describe the time intervals taken to flag errors during the memory read cycle.
#These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.
▲These parameters describe the time intervals taken to disable the CB and DB buses in preparation for a new data word during the memory read cycle.

PARAMETER MEASUREMENT INFORMATION

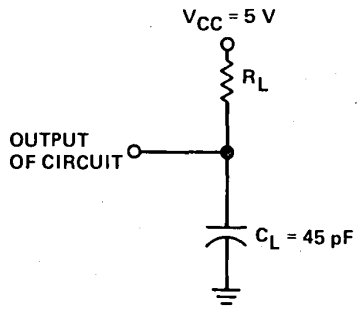

FIGURE 1–OUTPUT LOAD CIRCUIT

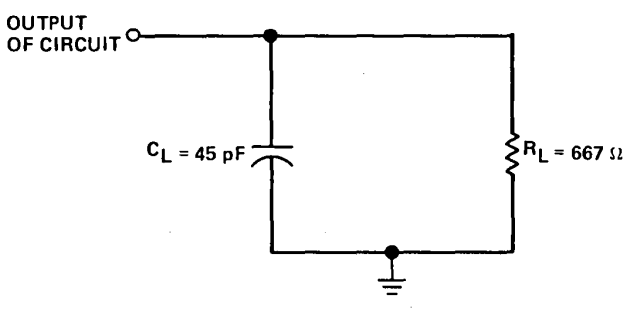

FIGURE 2–OUTPUT LOAD CIRCUIT

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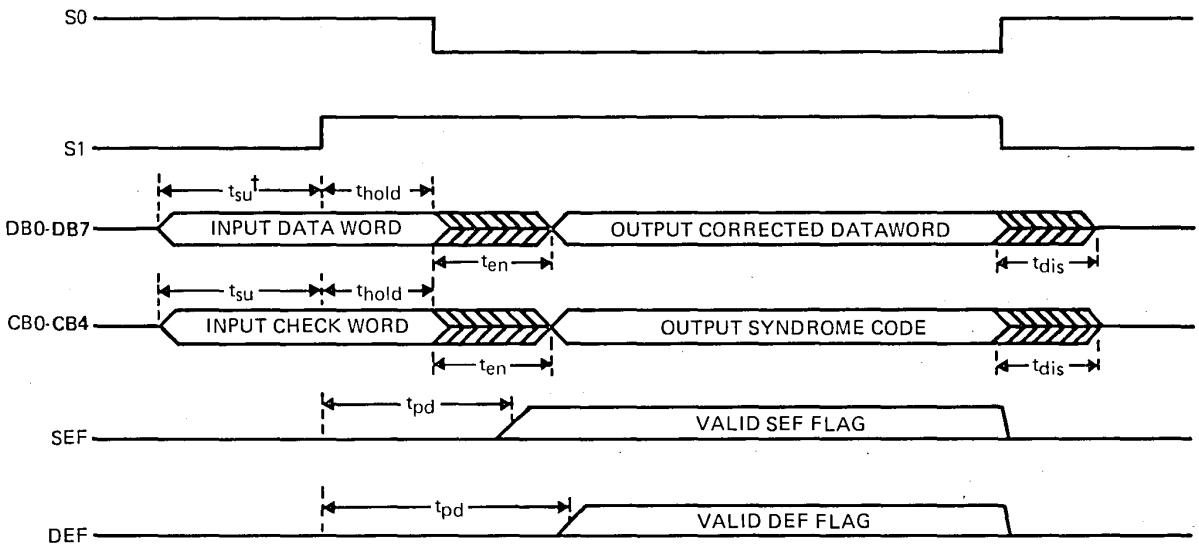
typical operating sequences

READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS



† NOTE: There are two conditions specified for t_{su} of Data or Checkword before S1↑. See recommended operating conditions for detail.