TYPES SN54LS589, SN74LS589
8-BIT SHIFT REGISTERS WITH INPUT LATCHES AND 3-STATE OUTPUT

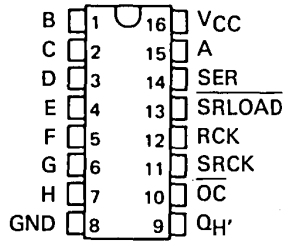
REVISED DECEMBER 1983

- **8-Bit Parallel Storage Register Inputs**
- **Shift Register has Direct Overriding Load and Power-Up Clear**
- **Guaranteed Shift Frequency . . . DC to 20 MHz**

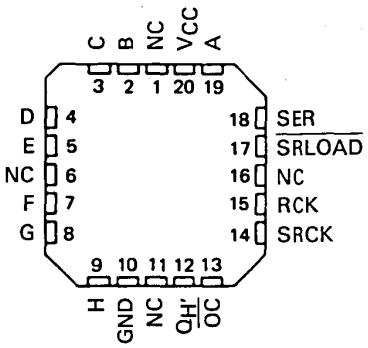
description

The 'LS589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register with 3-state outputs. Both the storage register and shift register have positive-edge triggered clocks. The shift register has a direct load (from storage) input.

SN54LS589 . . . J PACKAGE
SN74LS589 . . . J OR N PACKAGE
(TOP VIEW)



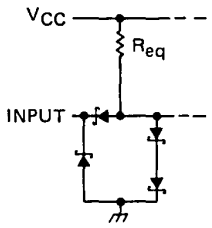
SN54LS589 . . . FK PACKAGE
SN74LS589 . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

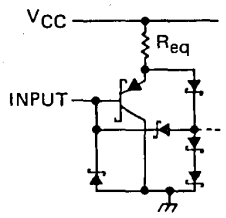
schematics of inputs and outputs

EQUIVALENT OF SERIAL AND DATA INPUTS



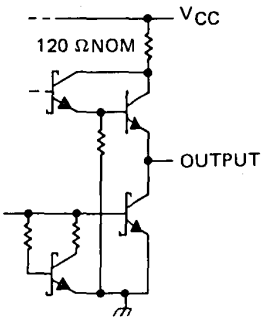
Serial: R_{eq} = 20 kΩ Nom
A thru H: R_{eq} = 25 kΩ Nom

EQUIVALENT OF ALL OTHER INPUTS



RCK, SRCK: R_{eq} = 10 kΩ Nom
All other: R_{eq} = 13 kΩ Nom

$Q_{H'}$ OUTPUT



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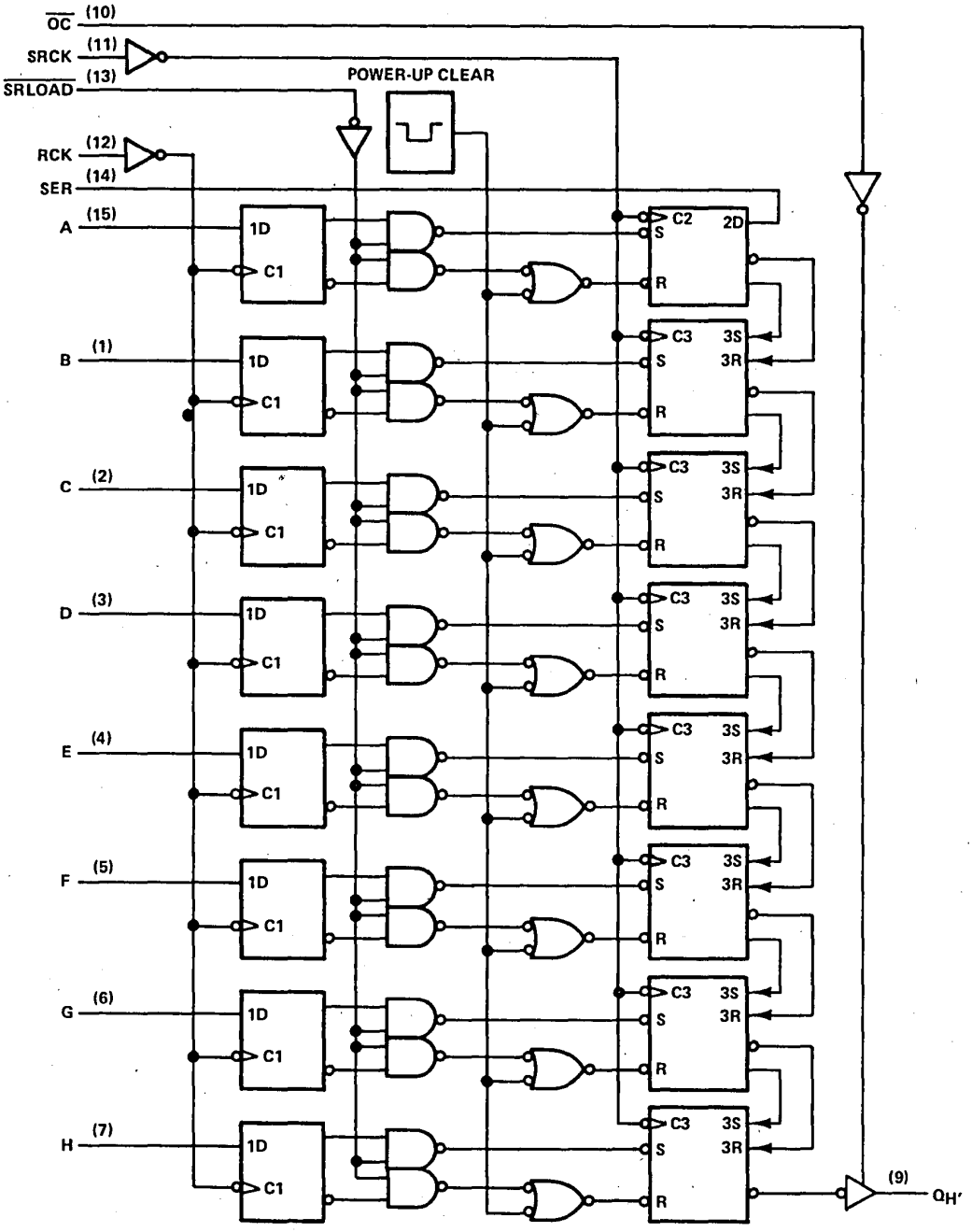
TTL DEVICES

logic diagram

'LS589



Pin numbers shown on logic notation are for J or N packages.

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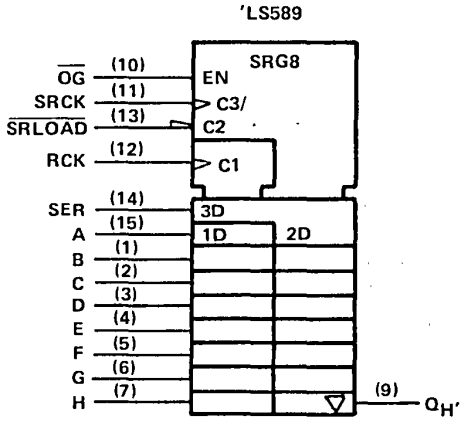
logic symbol†



Pin numbers shown on logic notation are for J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS589 . . . . . −55°C to 125°C
SN74LS589 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current					−1			−1	mA
I_{OL}	Low-level output current					8			16	mA
f_{SRCK}	Shift clock frequency			0		20	0		20	MHz
t_w	Pulse duration	SRCK	High	15			15			ns
			Low	35			35			
		RCK		20			20			
		$\overline{\text{SRLOAD}}$		40			40			
t_{su}	Setup time	Data before RCK ↑		20			20			ns
		SER before SRCK ↑		20			20			
		$\overline{\text{SRLOAD}}$ inactive before SRCK ↑		30			30			
		RCK ↑ before $\overline{\text{SRLOAD}}$ ↑ (see Note 2)		40			40			
t_h	Hold time	Data after RCK ↑		0			0			ns
		SER after SRCK ↑		0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

NOTE 2: The RCK ↑ to $\overline{\text{SRLOAD}}$ setup time ensures the data saved by RCK ↑ will also be loaded into the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = – 18 mA				– 1.5			– 1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = – 1 mA		2.4	3.2		2.4	3.2		V
V_{OL}		V_{CC} = MIN	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA					0.35	0.5	
I_{OZH}		V_{CC} = MAX, V_O = 2.7 V				20			20	μA
I_{OZL}		V_{CC} = MAX, V_O = 0.4 V				– 0.2			– 0.2	mA
I_{IL}		V_{CC} = MAX, V_I = 7 V				– 0.1			– 0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	SER, A → H	V_{CC} = MAX, V_I = 0.4 V				– 0.4			– 0.4	mA
	Others					– 0.2			– 0.2	
I_{OS}§		V_{CC} = MAX, V_O = 0 V		– 20		– 100	– 20		– 100	mA
I_{CC}	I_{CCH}	V_{CC} = MAX,			30	45		30	45	mA
	I_{CCL}	All possible inputs grounded,			30	45		30	45	
	I_{CCZ}	Output open			35	53		35	53	

† For conditions shown as MIN or MAX use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS589			UNIT
				MIN	TYP	MAX	
f_{max}	SRCK			20	35		MHz
t_{PLH}	SRCK↑	Q_H'	R_L = 1 kΩ, C_L = 30 pf		15	23	ns
t_{PHL}					20	30	
t_{PLH}	$\overline{SRLOAD}$↓	Q_H'			38	57	ns
t_{PHL}					29	44	
t_{PLH}	RCK↑	Q_H'	R_L = 1 kΩ, C_L = 30 pf, $\overline{SRLOAD}$ = L		41	60	ns
t_{PHL}					32	48	
t_{PZH}	$\overline{OC}$	Q_H'	R_L = 667 Ω, C_L = 5 pf		10	15	ns
t_{PZL}					18	27	
t_{PHZ}					20	30	
t_{PLZ}					20	30	

NOTE 2: See General Information Section for load circuits and voltage waveforms.

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timing diagram

'LS589