

## 8255A, 8255A-5

### *Programmable Peripheral Interface*

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

#### **Rochester Electronics Manufactured Components**

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Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

#### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*



# 8255A/8255A-5 PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range
- 40 Pin DIP Package

(See Intel Packaging: Order Number: 240800-001, Package Type P)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmable in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

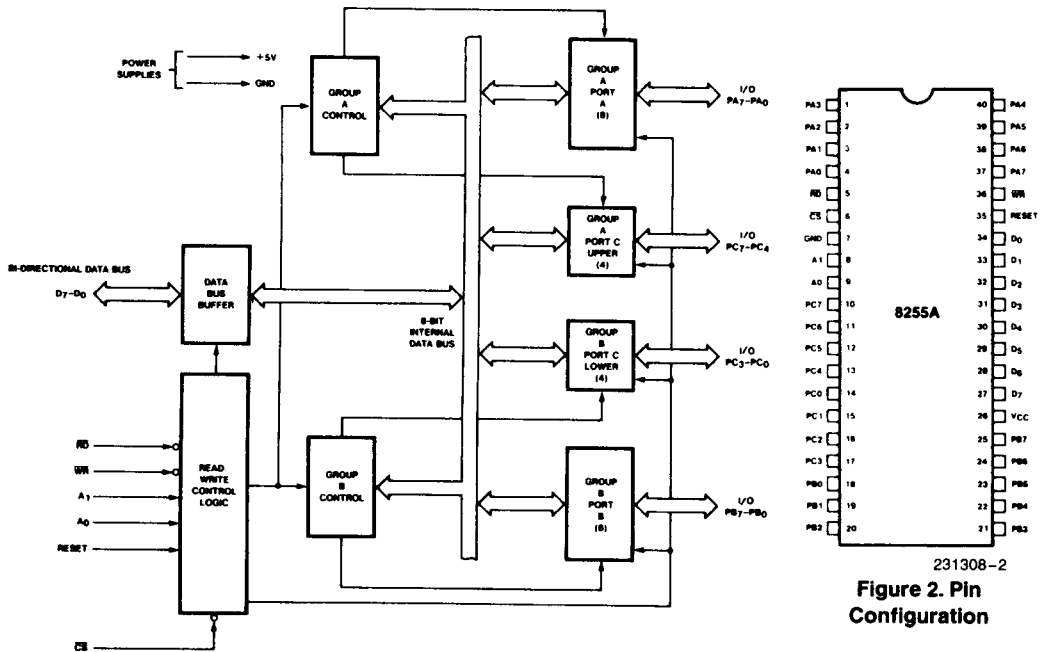


Figure 1. 8255A Block Diagram

Figure 2. Pin Configuration

## 8255A FUNCTIONAL DESCRIPTION

### General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

### Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

### Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the

CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

### ( $\overline{CS}$ )

**Chip Select.** A "low" on this input pin enables the communication between the 8255A and the CPU.

### ( $\overline{RD}$ )

**Read.** A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

### ( $\overline{WR}$ )

**Write.** A "low" on this input pin enables the CPU to write data or control words into the 8255A.

### ( $A_0$ and $A_1$ )

**Port Select 0 and Port Select 1.** These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus ( $A_0$  and  $A_1$ ).

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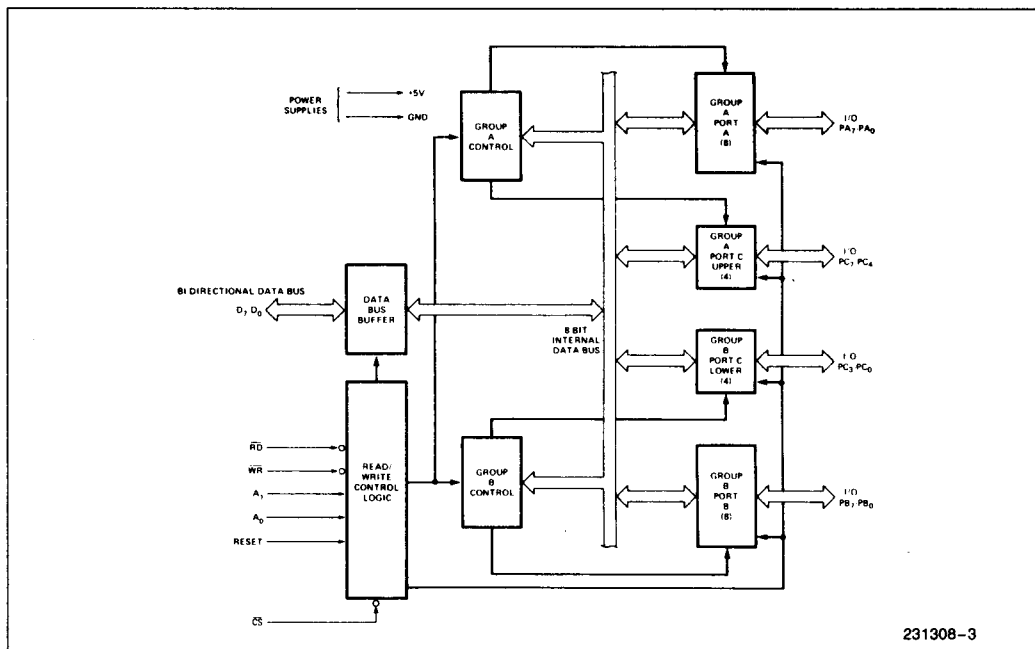


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

## 8255A BASIC OPERATION

A <sub>1</sub>	A <sub>0</sub>	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					<b>Output Operation (WRITE)</b>
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					<b>Disable Function</b>
X	X	X	X	1	Data Bus → 3-State
1	1	0	1	0	Illegal Condition
X	X	1	1	0	Data Bus → 3-State

### (RESET)

**Reset.** A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

### Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A—Port A and Port C upper (C7–C4)

Control Group B—Port B and Port C lower (C3–C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

### Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

**Port A.** One 8-bit data output latch/buffer and one 8-bit data input latch.

**Port B.** One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

**Port C.** One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

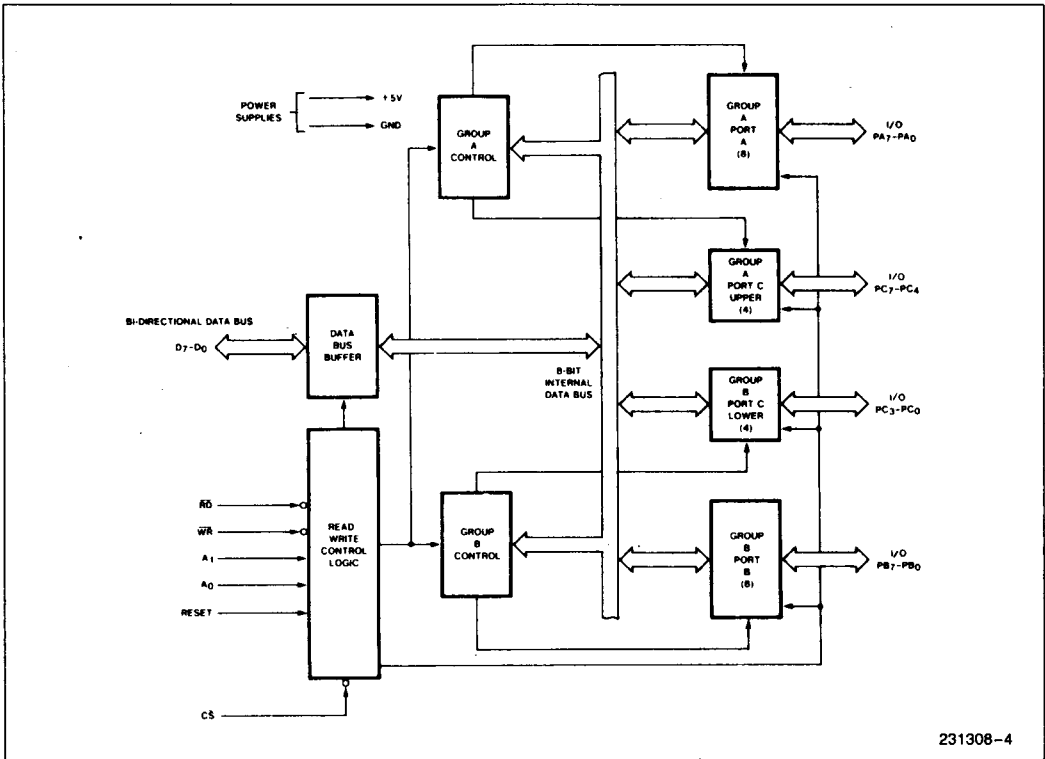
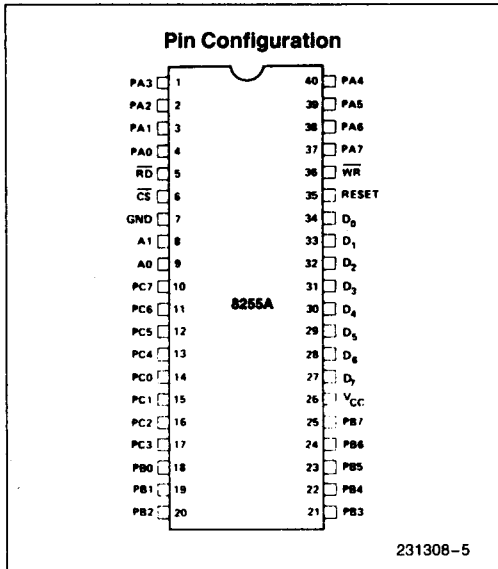


Figure 4. 8255A Block Diagram Showing Group A and Group B Control Functions



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Pin Names

D7-D0	Data Bus (Bi-Directional)
RESET	Reset Input
CS	Chip Select
RD	Read Input
WR	Write Input
A0, A1	Port Address
PA7-PA0	Port A (BIT)
PB7-PB0	Port B (BIT)
PC7-PC0	Port C (BIT)
VCC	+ 5 Volts
GND	0 Volts

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0—Basic Input/Output

Mode 1—Strobed Input/Output

Mode 2—Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

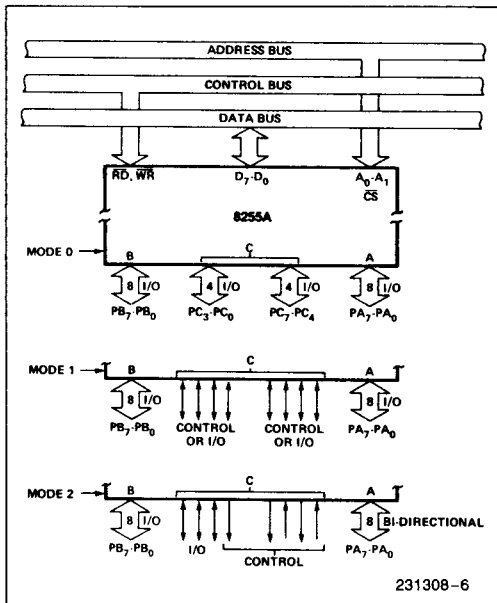


Figure 5. Basic Mode Definitions and Bus Interface

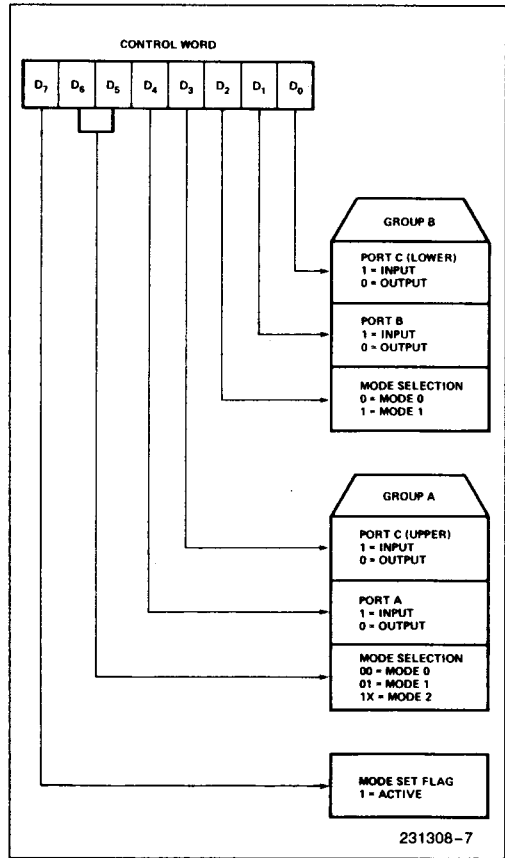


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

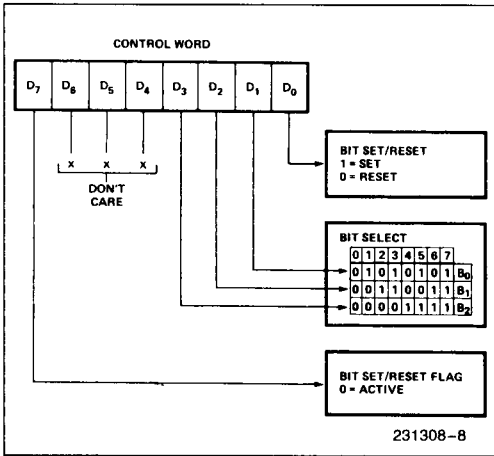


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

### Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is set—Interrupt enable

(BIT-RESET)—INTE is RESET—Interrupt disable

**NOTE:**

All Mask flip-flops are automatically reset during mode selection and device Reset.

### Operating Modes

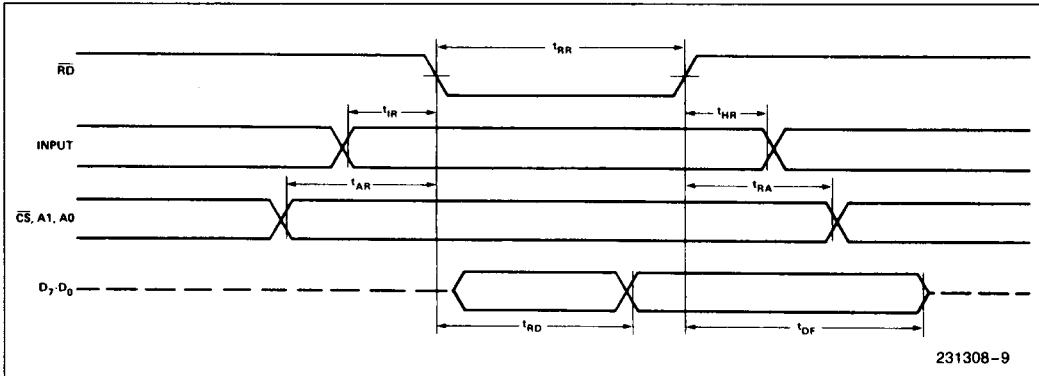
**MODE 0 (Basic Input/Output).** This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

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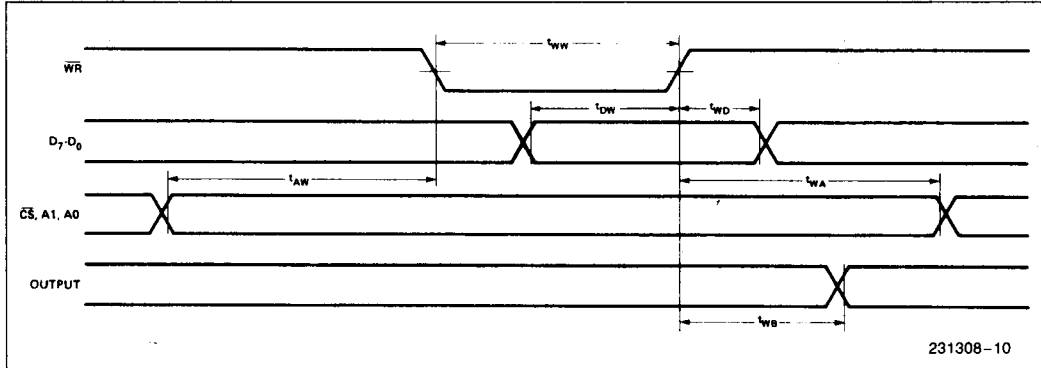
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

### MODE 0 (BASIC INPUT)



**MODE 0 (BASIC OUTPUT)**



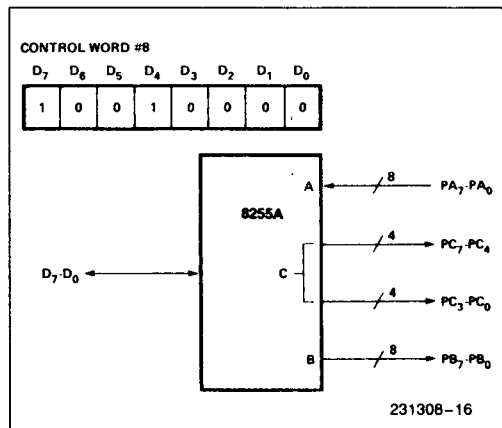
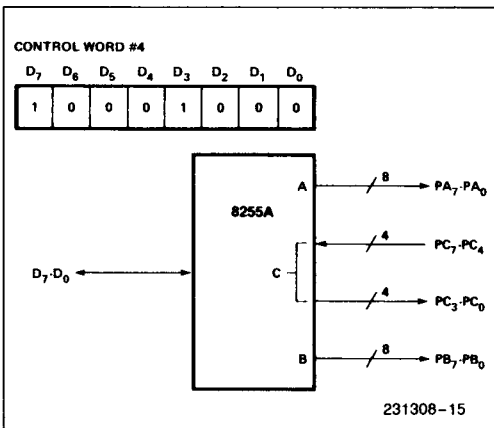
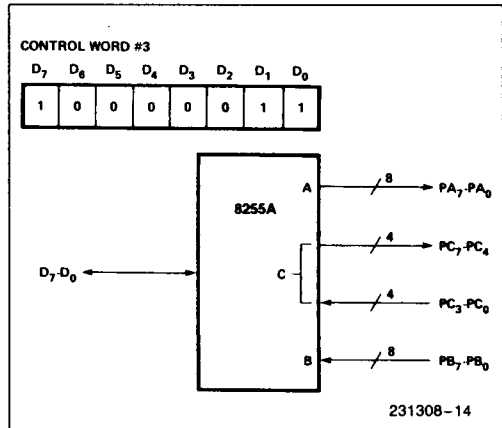
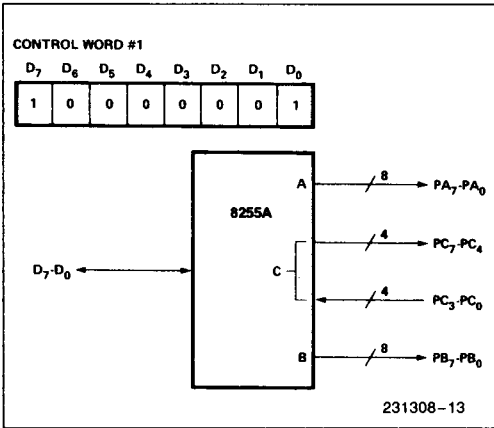
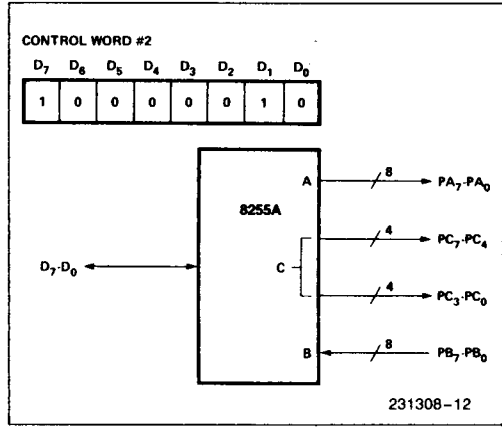
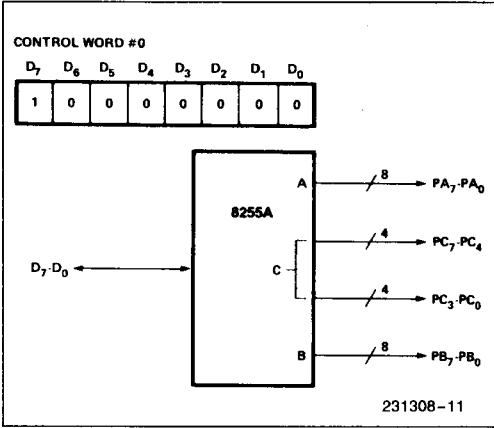
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**MODE 0 PORT DEFINITION**

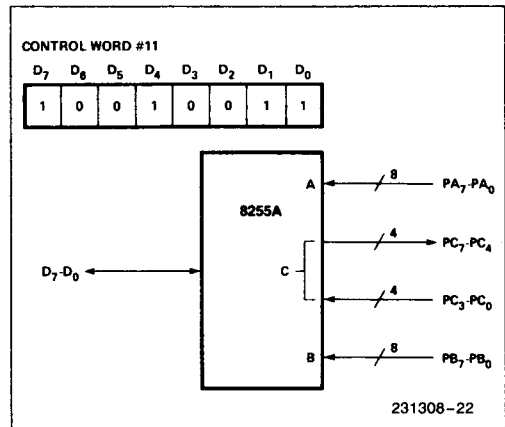
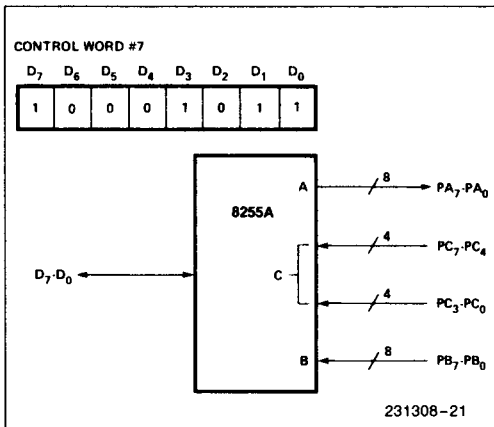
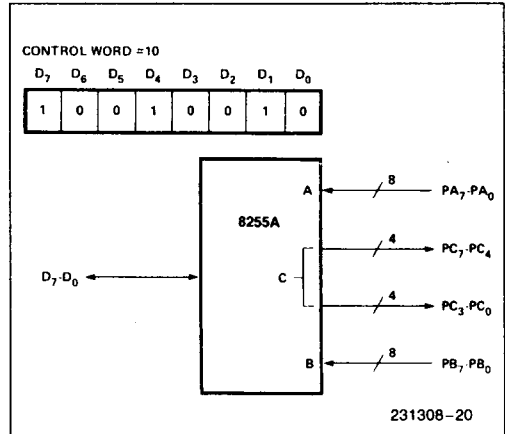
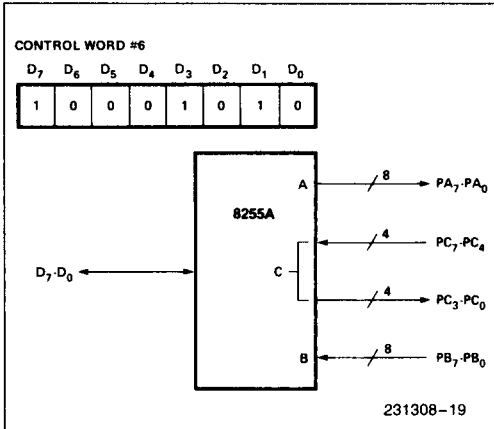
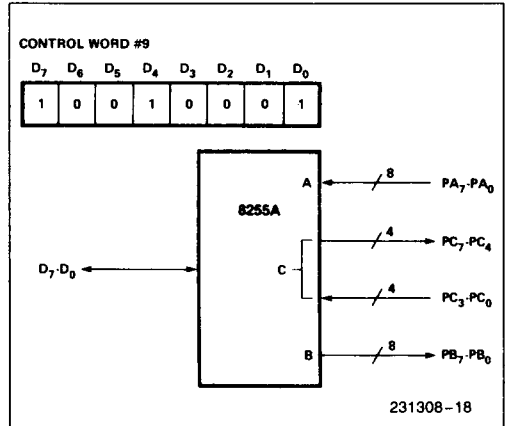
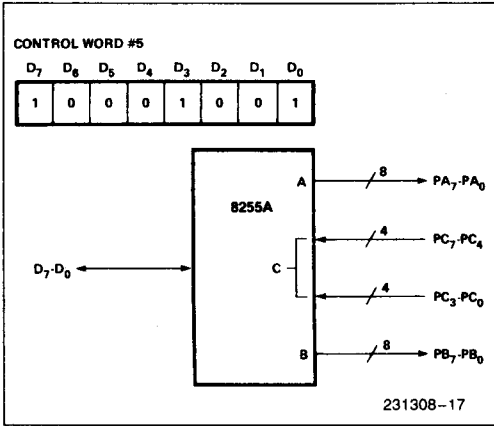
A		B		Group A			Group B	
D <sub>4</sub>	D <sub>3</sub>	D <sub>1</sub>	D <sub>0</sub>	Port A	Port C (Upper)	#	Port B	Port C (Lower)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

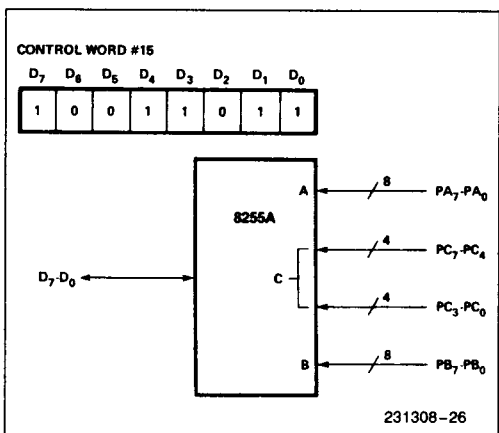
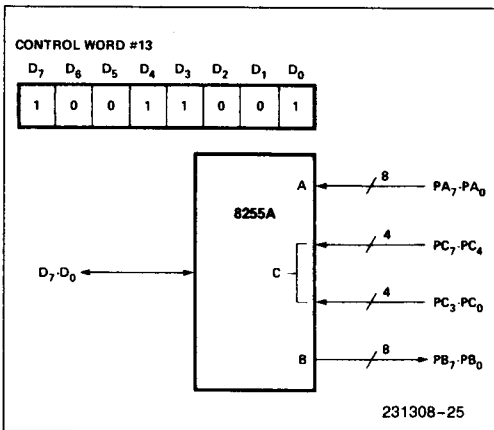
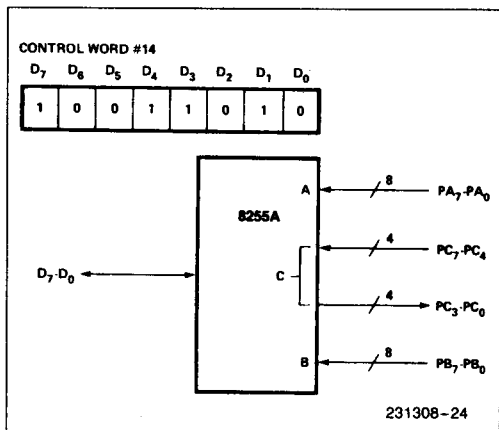
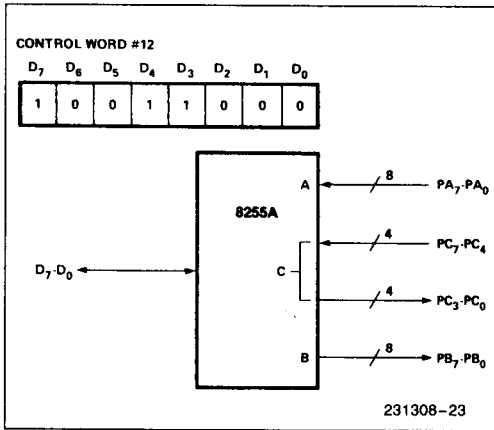


MODE CONFIGURATIONS



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### Operating Modes

**MODE 1 (Strobed Input/Output).** This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

### Input Control Signal Definition

**STB (Strobe Input).** A "low" on this input loads data into the input latch.

### IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

### INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

**INTE A**

Controlled by bit set/reset of PC<sub>4</sub>.

**INTE B**

Controlled by bit set/reset of PC<sub>2</sub>.

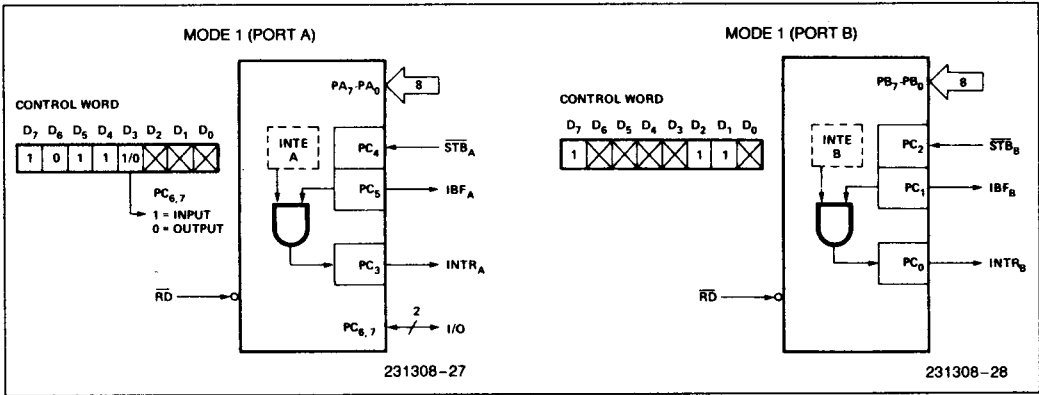


Figure 8. MODE 1 Input

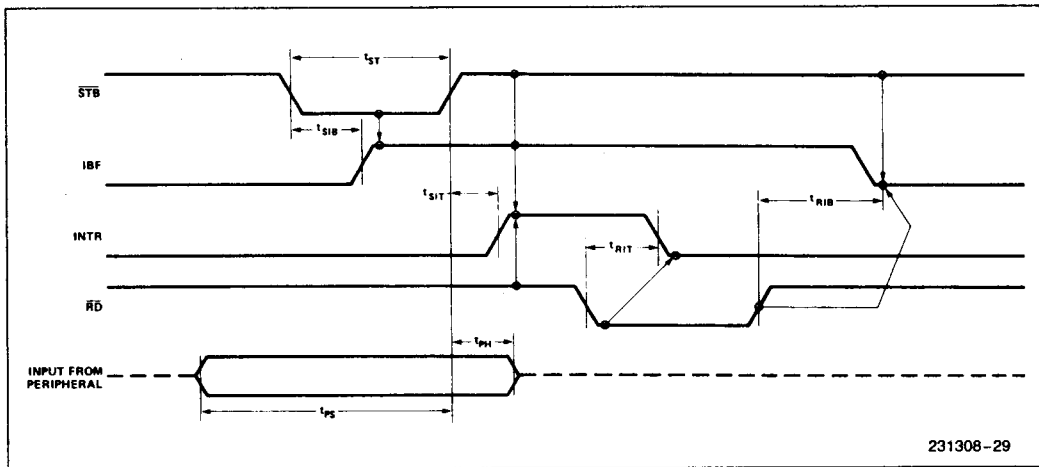


Figure 9. MODE 1 (Strobed Input)

### Output Control Signal Definition

**$\overline{OBF}$  (Output Buffer Full F/F).** The  $\overline{OBF}$  output will go "low" to indicate that the CPU has written data out to the specified port. The  $\overline{OBF}$  F/F will be set by the rising edge of the  $\overline{WR}$  input and reset by  $\overline{ACK}$  input being low.

**$\overline{ACK}$  (Acknowledge Input).** A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

**INTR (Interrupt Request).** A "high" on this output can be used to interrupt the CPU when an output

device has accepted data transmitted by the CPU. INTR is set when  $\overline{ACK}$  is a "one",  $\overline{OBF}$  is a "one", and INTE is a "one". It is reset by the falling edge of  $\overline{WR}$ .

#### INTE A

Controlled by bit set/reset of PC<sub>6</sub>.

#### INTE B

Controlled by bit set/reset of PC<sub>2</sub>.

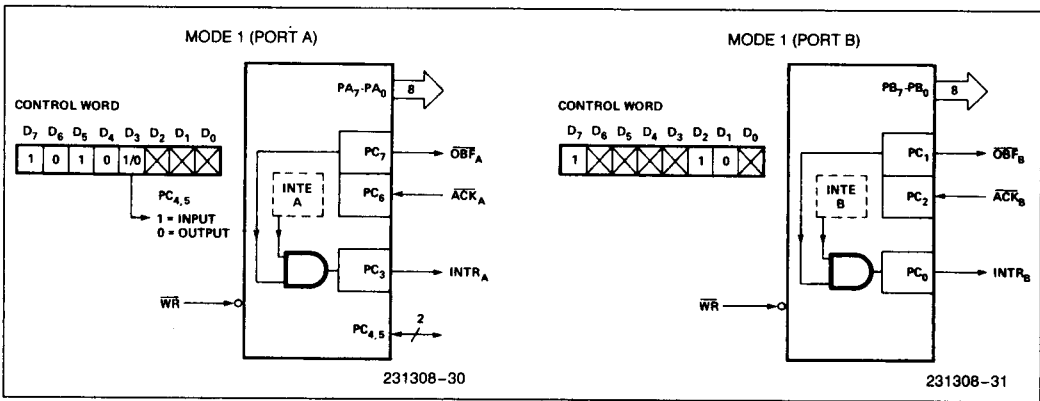


Figure 10. MODE 1 Output

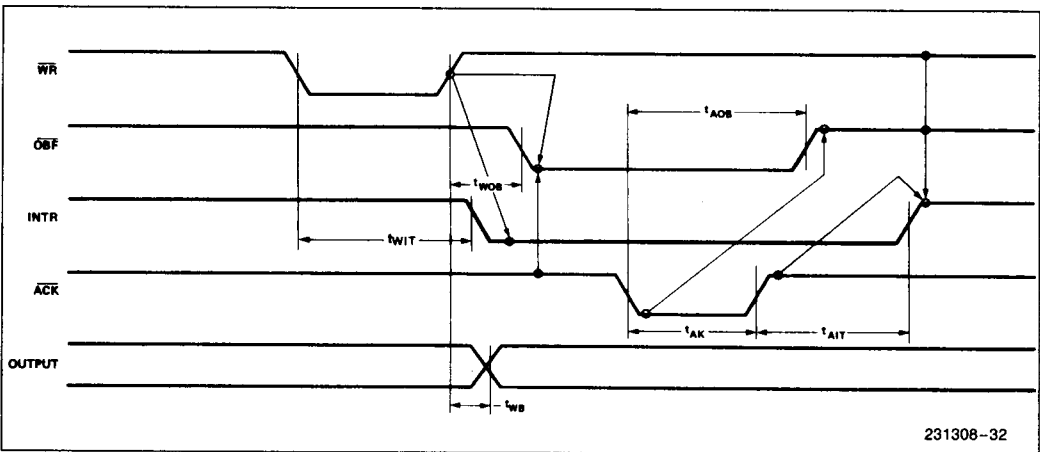


Figure 11. MODE 1 (Strobed Output)

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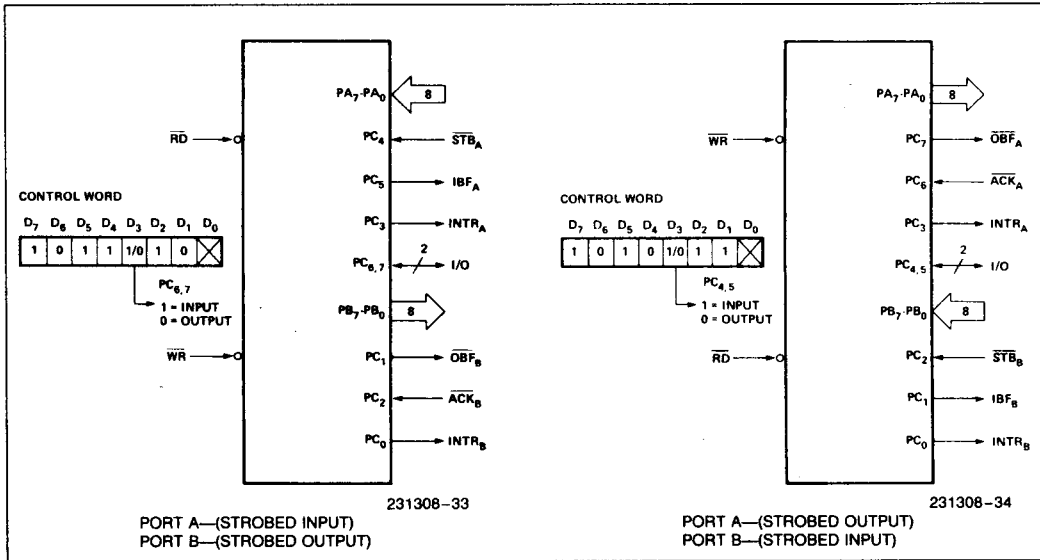


Figure 12. Combinations of MODE 1

**Combinations of MODE 1**

Port A and Port B can be individually defined as input or output in MODE 1 to support a wide variety of strobed I/O applications.

**Operating Modes**

**MODE 2 (Strobed Bidirectional Bus I/O).** This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

**Bidirectional Bus I/O Control Signal Definition**

**INTR (Interrupt Request).** A high on this output can be used to interrupt the CPU for both input or output operations.

**Output Operations**

**OBF (Output Buffer Full).** The OBF output will go "low" to indicate that the CPU has written data out to port A.

**ACK (Acknowledge).** A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

**INTE 1 (The INTE Flip-Flop Associated with OBF).** Controlled by bit set/reset of PC<sub>6</sub>.

**Input Operations**

**STB (Strobe Input).** A "low" on this input loads data into the input latch.

**IBF (Input Buffer Full F/F).** A "high" on this output indicates that data has been loaded into the input latch.

**INTE 2 (The INTE Flip-Flop Associated with IBF).** Controlled by bit set/reset of PC<sub>4</sub>.

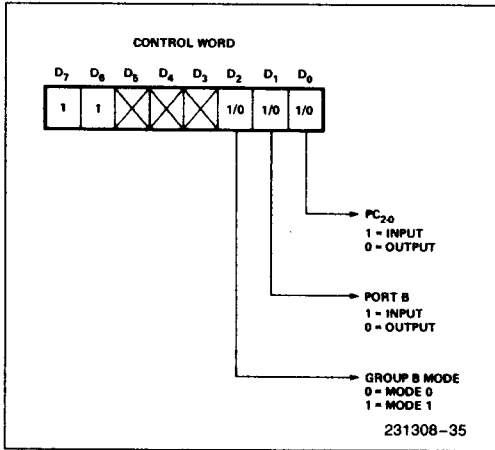


Figure 13. MODE Control Word

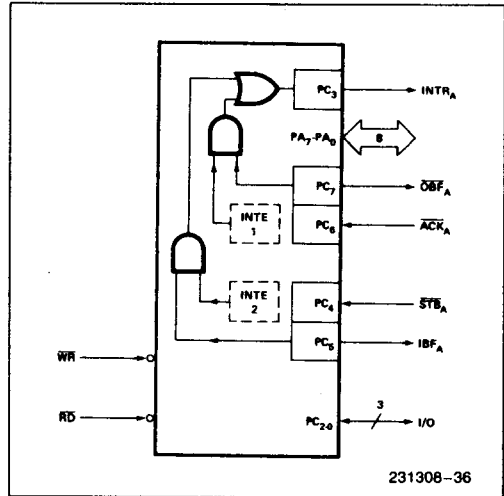
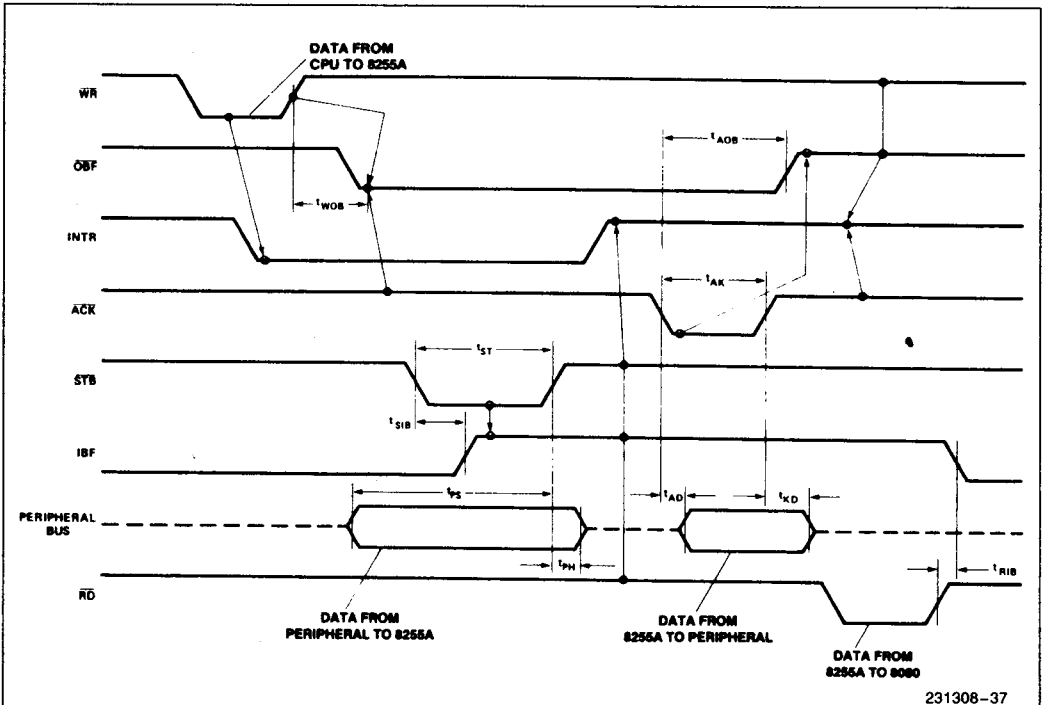


Figure 14. MODE 2

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**NOTE:**  
Any sequence where  $\overline{WR}$  occurs before  $\overline{ACK}$  and  $\overline{STB}$  occurs before  $\overline{RD}$  is permissible.  
( $\overline{INTR} = \overline{IBF} \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$ )

Figure 15. MODE 2 (Bidirectional)

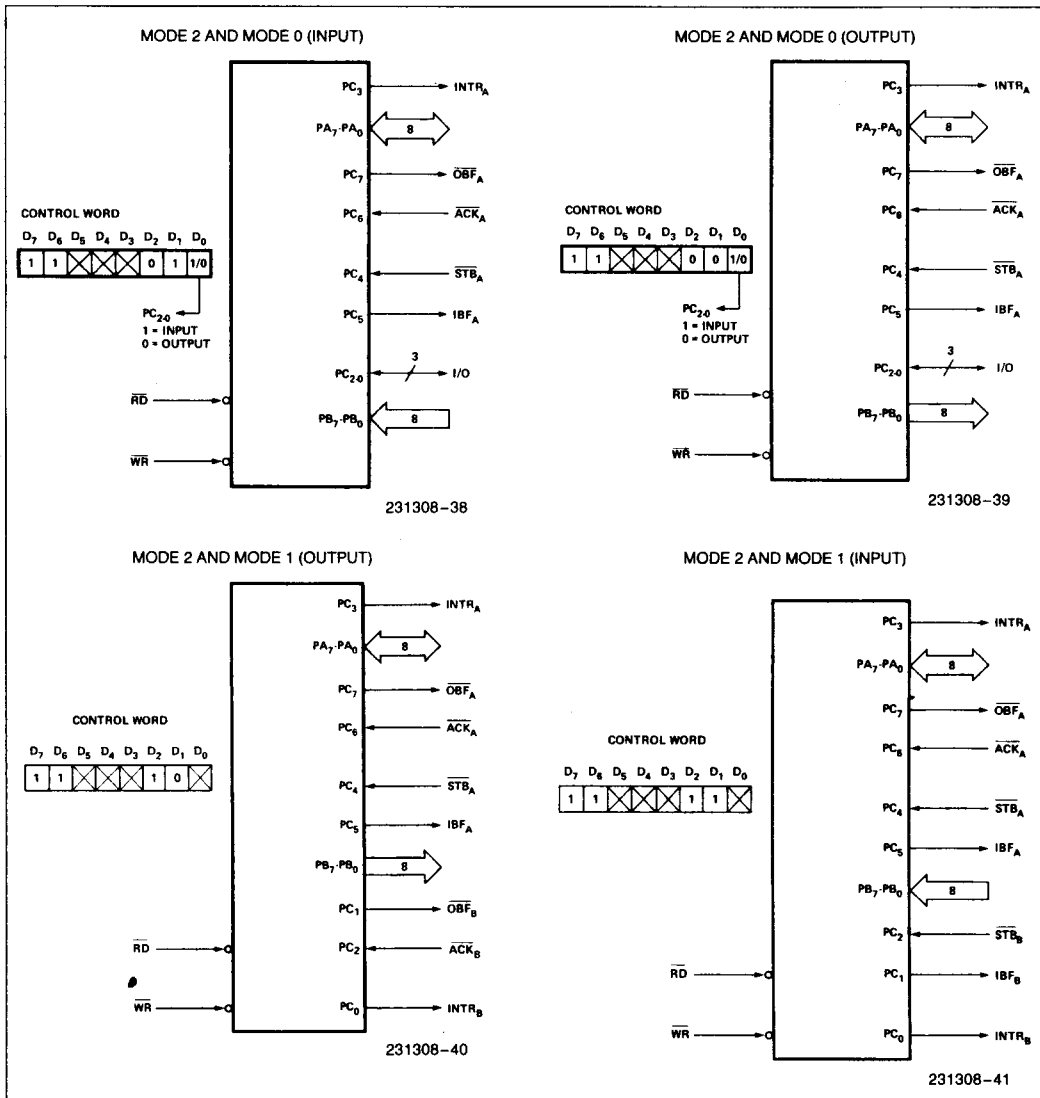


Figure 16. MODE 1/4 Combinations



**Mode Definition Summary**

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA <sub>0</sub>	IN	OUT	IN	OUT	↔
PA <sub>1</sub>	IN	OUT	IN	OUT	↔
PA <sub>2</sub>	IN	OUT	IN	OUT	↔
PA <sub>3</sub>	IN	OUT	IN	OUT	↔
PA <sub>4</sub>	IN	OUT	IN	OUT	↔
PA <sub>5</sub>	IN	OUT	IN	OUT	↔
PA <sub>6</sub>	IN	OUT	IN	OUT	↔
PA <sub>7</sub>	IN	OUT	IN	OUT	↔
PB <sub>0</sub>	IN	OUT	IN	OUT	—
PB <sub>1</sub>	IN	OUT	IN	OUT	—
PB <sub>2</sub>	IN	OUT	IN	OUT	—
PB <sub>3</sub>	IN	OUT	IN	OUT	—
PB <sub>4</sub>	IN	OUT	IN	OUT	—
PB <sub>5</sub>	IN	OUT	IN	OUT	—
PB <sub>6</sub>	IN	OUT	IN	OUT	—
PB <sub>7</sub>	IN	OUT	IN	OUT	—
PC <sub>0</sub>	IN	OUT	INTR <sub>B</sub>	INTR <sub>B</sub>	I/O
PC <sub>1</sub>	IN	OUT	IBF <sub>B</sub>	OBFB	I/O
PC <sub>2</sub>	IN	OUT	STB <sub>B</sub>	ACK <sub>B</sub>	I/O
PC <sub>3</sub>	IN	OUT	INTR <sub>A</sub>	INTR <sub>A</sub>	INTR <sub>A</sub>
PC <sub>4</sub>	IN	OUT	STB <sub>A</sub>	I/O	STB <sub>A</sub>
PC <sub>5</sub>	IN	OUT	IBF <sub>A</sub>	I/O	IBF <sub>A</sub>
PC <sub>6</sub>	IN	OUT	I/O	ACK <sub>A</sub>	ACK <sub>A</sub>
PC <sub>7</sub>	IN	OUT	I/O	OBFA	OBFA

}  
 MODE 0  
 OR MODE 1  
 ONLY

3

**Special Mode Combination Considerations**

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs—

All input lines can be accessed during a normal Port C read.

If Programmed as Outputs—

Bits in C upper (PC<sub>7</sub>–PC<sub>4</sub>) must be individually accessed using the bit set/reset function.

Bits in C lower (PC<sub>3</sub>–PC<sub>0</sub>) can be accessed using the bit set/reset function or accessed as a three-some by writing into Port C.

This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

**Reading Port C Status**

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

**Source Current Capability on Port B and Port C**

Any set of eight output buffers, selected randomly from Ports B and C can source 1 mA at 1.5 volts.

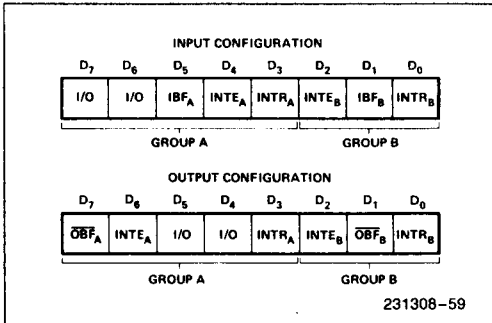


Figure 17. MODE 1 Status Word Format

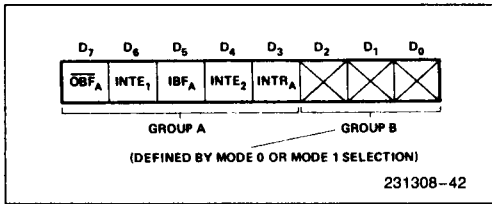


Figure 18. MODE 2 Status Word Format

**APPLICATIONS OF THE 8255A**

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 represent a few examples of typical applications of the 8255A.

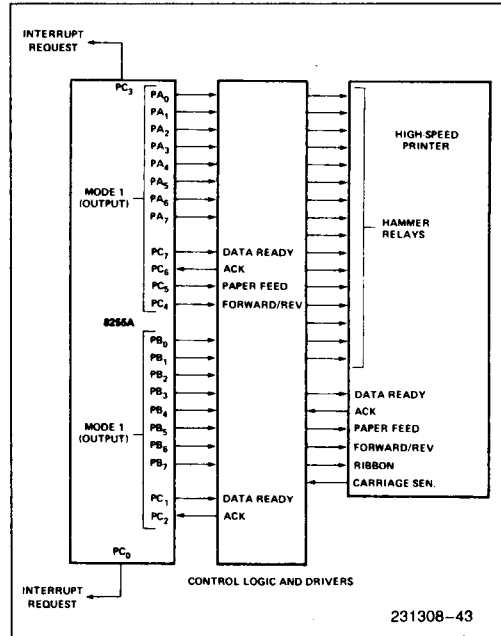


Figure 19. Printer Interface

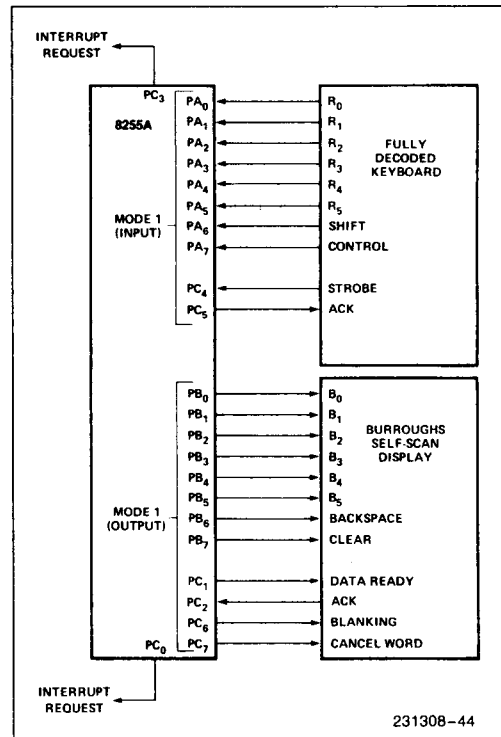


Figure 20. Keyboard and Display Interface

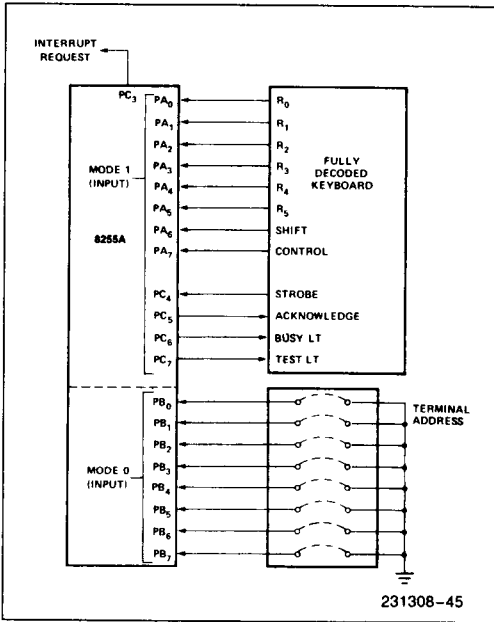


Figure 21. Keyboard and Terminal Address Interface

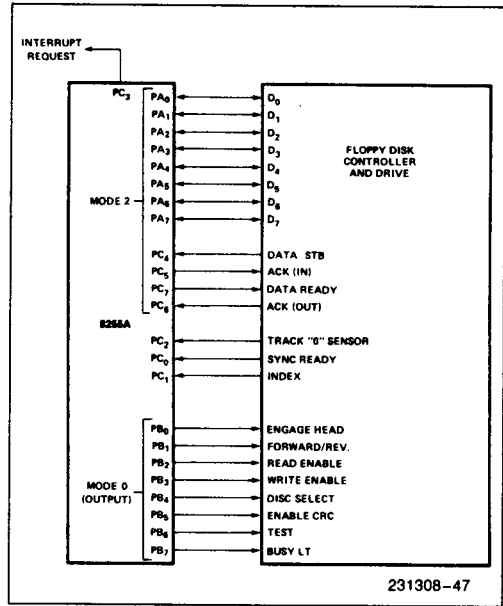


Figure 23. Basic Floppy Disk Interface

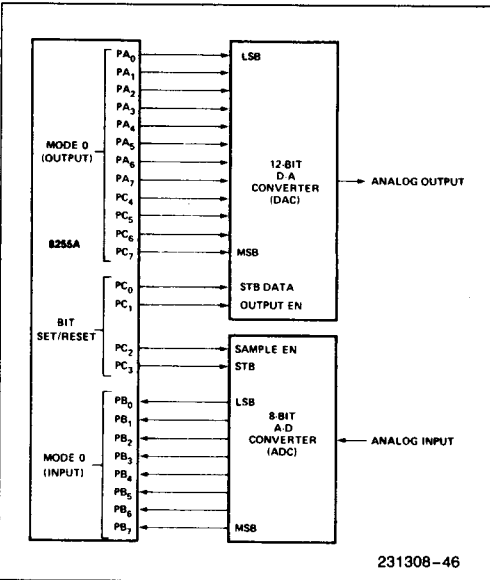


Figure 22. Digital to Analog, Analog to Digital

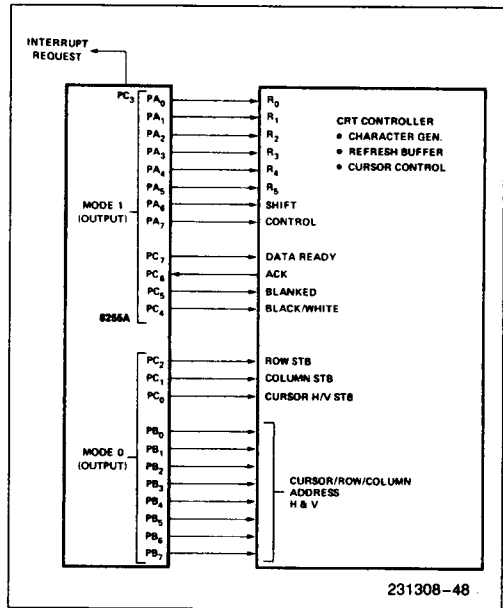


Figure 24. Basic CRT Controller Interface



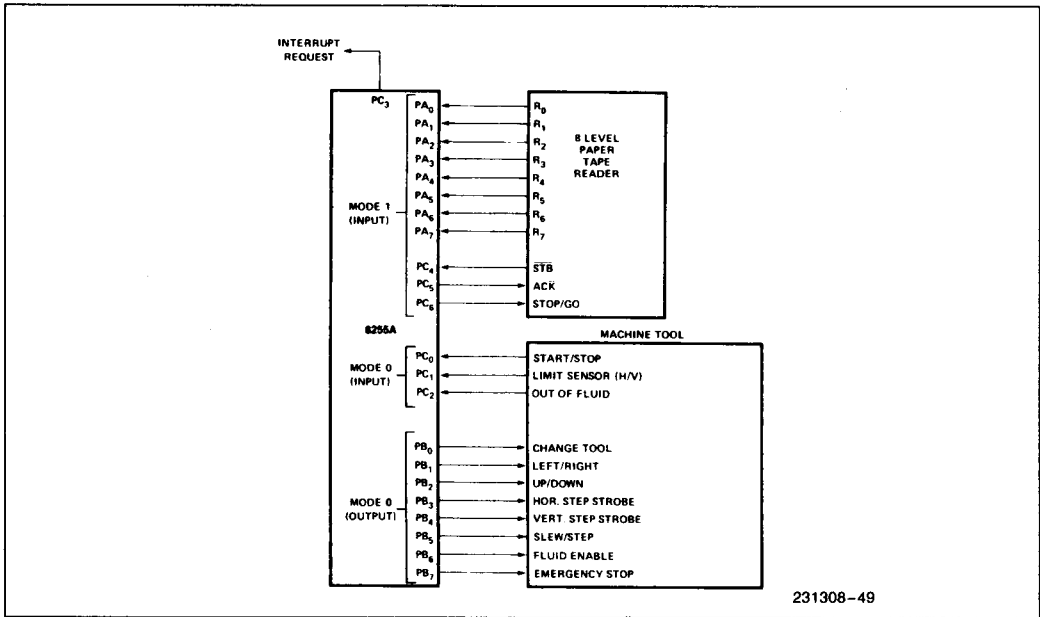


Figure 25. Machine Tool Controller Interface

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias . . . . . 0°C to 70°C  
 Storage Temperature . . . . . -65°C to +150°C  
 Voltage on Any Pin  
 with Respect to Ground . . . . . -0.5V to +7V  
 Power Dissipation . . . . . 1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**D.C. CHARACTERISTICS** T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = +5V ± 10%, GND = 0V\*

Symbol	Parameter	Min	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub>	V	
V <sub>OL</sub> (DB)	Output Low Voltage (Data Bus)		0.45*	V	I <sub>OL</sub> = 2.5 mA
V <sub>OL</sub> (PER)	Output Low Voltage (Peripheral Port)		0.45*	V	I <sub>OL</sub> = 1.7 mA
V <sub>OH</sub> (DB)	Output High Voltage (Data Bus)	2.4		V	I <sub>OH</sub> = -400 μA
V <sub>OH</sub> (PER)	Output High Voltage (Peripheral Port)	2.4		V	I <sub>OH</sub> = -200 μA
I <sub>DAR</sub> ( <sup>1</sup> )	Darlington Drive Current	-1.0	-4.0	mA	R <sub>EXT</sub> = 750Ω; V <sub>EXT</sub> = 1.5V
I <sub>CC</sub>	Power Supply Current		120	mA	
I <sub>IL</sub>	Input Load Current		± 10	μA	V <sub>IN</sub> = V <sub>CC</sub> to 0V
I <sub>OFL</sub>	Output Float Leakage		± 10	μA	V <sub>OUT</sub> = V <sub>CC</sub> to 0.45V

**NOTE:**

1. Available on any 8 pins from Port B and C.

**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$ 

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$C_{IN}$	Input Capacitance			10	pF	$f_c = 1\text{ MHz}^{(4)}$
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND <sup>(4)</sup>

**A.C. CHARACTERISTICS**  $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ ,  $\text{GND} = 0\text{V}^*$ 
**Bus Parameters**
**READ**

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
$t_{AR}$	Address Stable before READ	0		0		ns
$t_{RA}$	Address Stable after READ	0		0		ns
$t_{RR}$	READ Pulse Width	300		300		ns
$t_{RD}$	Data Valid from READ <sup>(1)</sup>		250		200	ns
$t_{DF}$	Data Float after READ	10	150	10	100	ns
$t_{RV}$	Time between READs and/or WRITEs	850		850		ns

**3**
**WRITE**

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
$t_{AW}$	Address Stable before WRITE	0		0		ns
$t_{WA}$	Address Stable after WRITE	20		20		ns
$t_{WW}$	WRITE Pulse Width	400		300		ns
$t_{DW}$	Data Valid to WRITE (T.E.)	100		100		ns
$t_{WD}$	Data Valid after WRITE	30		30		ns

**OTHER TIMINGS**

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
$t_{WB}$	WR = 1 to Output <sup>(1)</sup>		350		350	ns
$t_{IR}$	Peripheral Data before RD	0		0		ns
$t_{HR}$	Peripheral Data after RD	0		0		ns
$t_{AK}$	ACK Pulse Width	300		300		ns
$t_{ST}$	STB Pulse Width	500		500		ns
$t_{PS}$	Per. Data before T.E. of STB	0		0		ns
$t_{PH}$	Per. Data after T.E. of STB	180		180		ns
$t_{AD}$	ACK = 0 to Output <sup>(1)</sup>		300		300	ns
$t_{KD}$	ACK = 1 to Output Float	20	250	20	250	ns

**A.C. CHARACTERISTICS** (Continued)

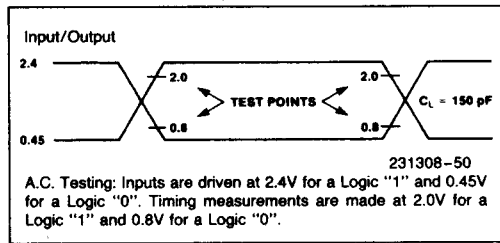
**OTHER TIMINGS** (Continued)

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
$t_{WOB}$	WR = 1 to OBF = 0 <sup>(1)</sup>		650		650	ns
$t_{AOB}$	ACK = 0 to OBF = 1 <sup>(1)</sup>		350		350	ns
$t_{SIB}$	STB = 0 to IBF = 1 <sup>(1)</sup>		300		300	ns
$t_{RIB}$	RD = 1 to IBF = 0 <sup>(1)</sup>		300		300	ns
$t_{RIT}$	RD = 0 to INTR = 0 <sup>(1)</sup>		400		400	ns
$t_{SIT}$	STB = 1 to INTR = 1 <sup>(1)</sup>		300		300	ns
$t_{AIT}$	ACK = 1 to INTR = 1 <sup>(1)</sup>		350		350	ns
$t_{WIT}$	WR = 0 to INTR = 0 <sup>(1,3)</sup>		850		850	ns

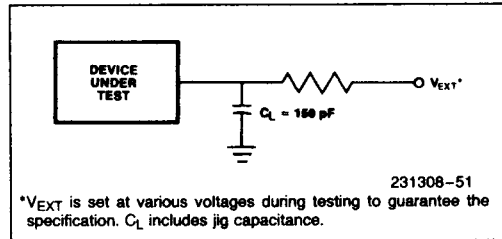
**NOTES:**

1. Test Conditions:  $C_L = 150$  pF.
  2. Period of Reset pulse must be at least 50  $\mu$ s during or after power on. Subsequent Reset pulse can be 500 ns min.
  3. INTR  $\uparrow$  may occur as early as WR  $\downarrow$ .
  4. Sampled, not 100% tested.
- \*For Extended Temperature EXPRESS, use M8255A electrical parameters.

**A.C. TESTING INPUT, OUTPUT WAVEFORM**

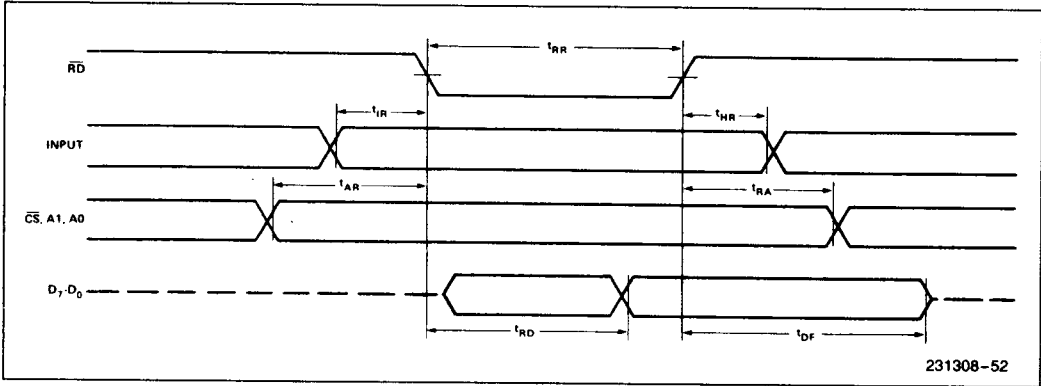


**A.C. TESTING LOAD CIRCUIT**

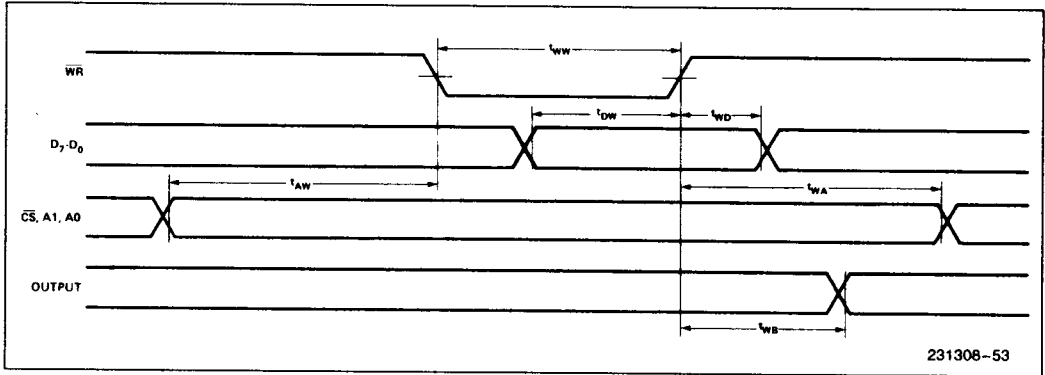


WAVEFORMS

MODE 0 (BASIC INPUT)



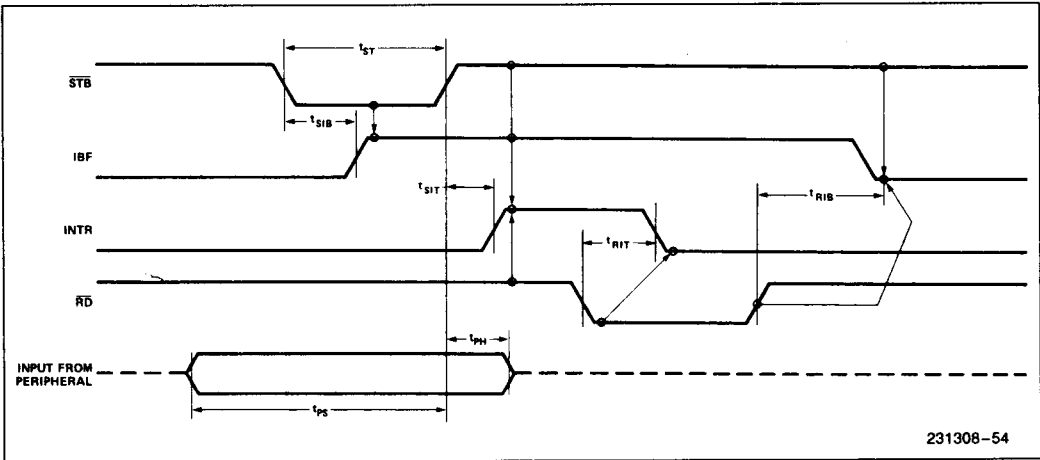
MODE 0 (BASIC OUTPUT)



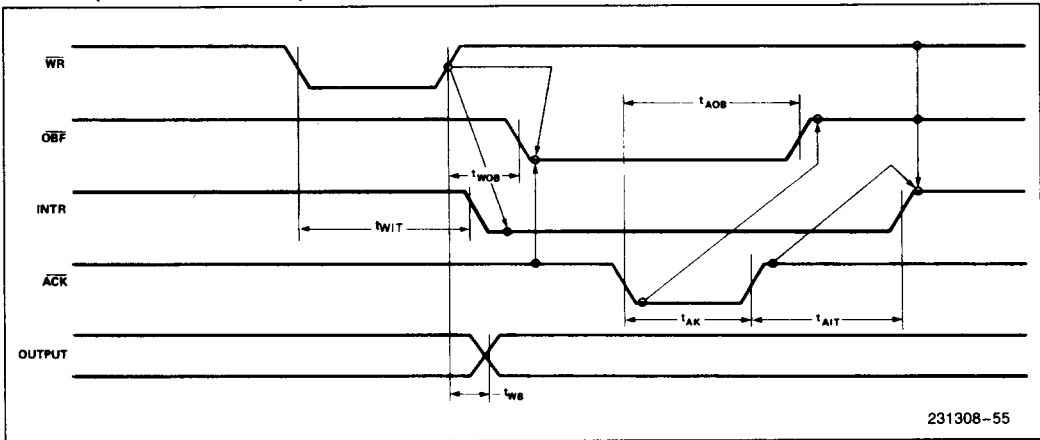
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**WAVEFORMS** (Continued)

**MODE 1 (STROBED INPUT)**



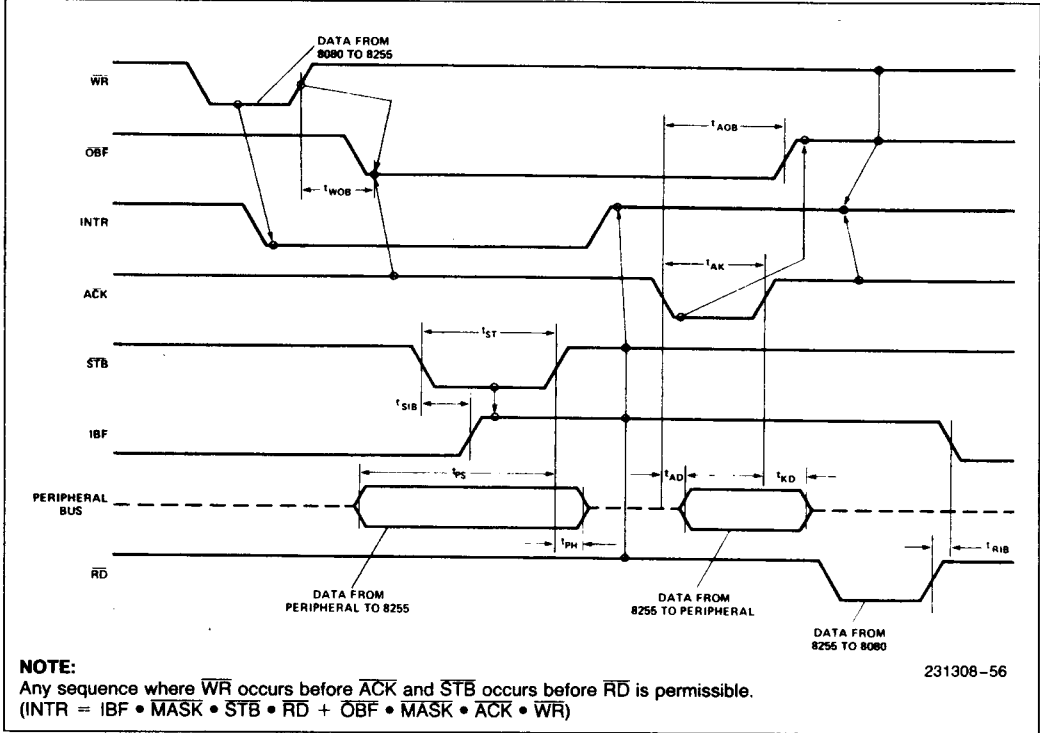
**MODE 1 (STROBED OUTPUT)**





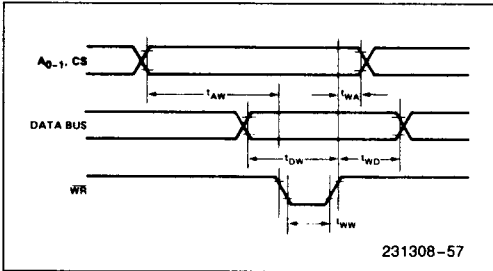
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)



3

WRITE TIMING



READ TIMING

